Delson
Technology Co, Ltd.

D916764B24QCD
64M x 64 HIGH PERFORMANCE UNBUFFERED DDR2 SDRAM SODIMM

Features

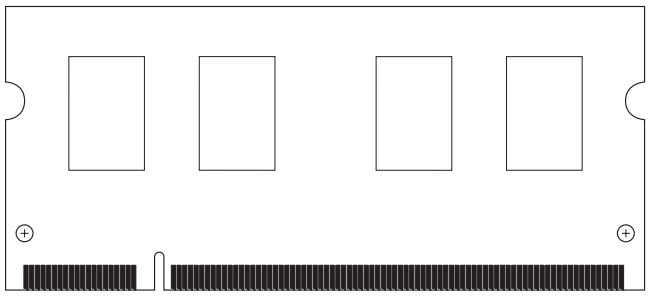
- 200-pin, unbuffered small outline, dual in-line memory module (SODIMM)
- JEDEC standard 1.8V ± 0.1V power supply
- VDDQ=1.8V ± 0.1V
- Fast data transfer rate:PC2-4200, or PC2-5300, or PC2-6400
- Programmable CAS Latency(CL): 3, 4, 5 for DDR2-400/533/667/800(G5). 4, 5, 6 for DDR2-800(G6)
- Programmable Additive Latency (AL): 0, 1, 2, 3, 4 and 5
- Write Latency(WL) = Read Latency (RL)-1
- Programmble burst lengths: 4 or 8
- Differential data strobe (DQS, DQS#) (Single ended data strobe option)
- On-die termination (ODT)
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- Serial Presence Detect (SPD) with EEPROM

Description

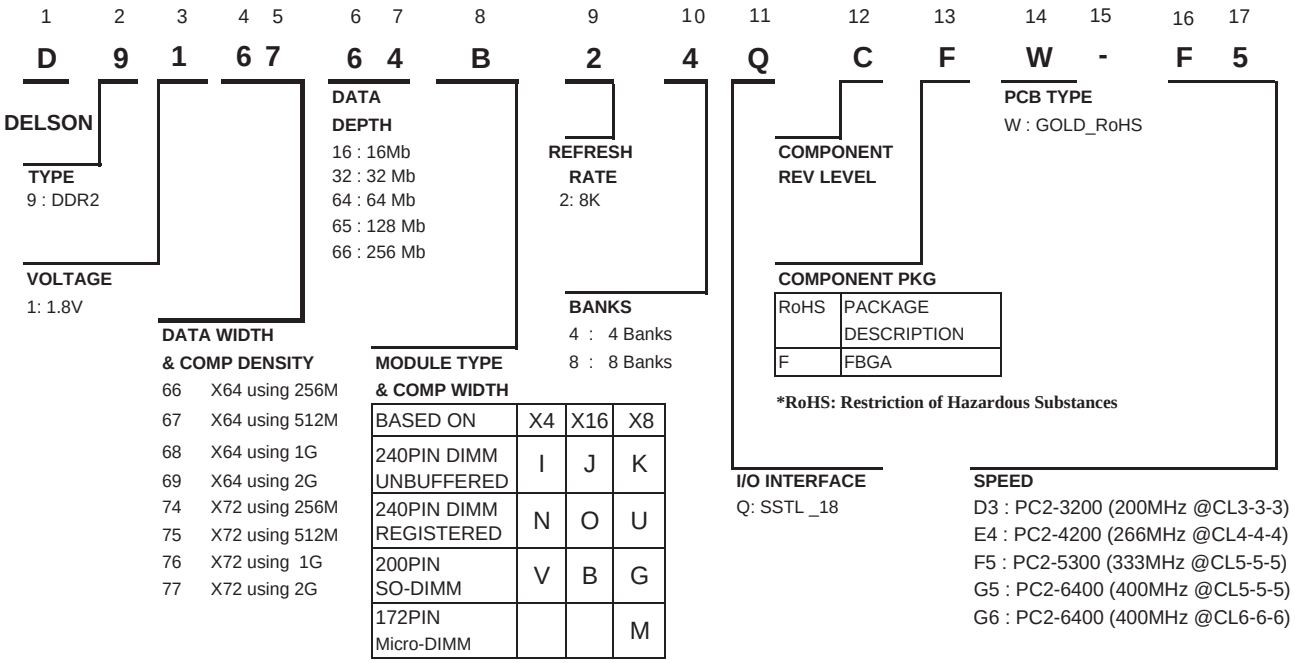
The D916764B24QC memory module is organized as 67,108,864 x 64 bits in a 200 pin memory module. The 64M x 64 memory module uses 4 ProMOS 64M x 16 DDR2 SDRAMs. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

Speed Grade

	DDR2-533 PC2-4200 (E4)	DDR2-667 PC2-5300 (F5)	DDR2-800 PC2-6400 (G6)	Units
Bandwith@CL=4	533	533	533	Mbps
Bandwith@CL=5	533	667	667	Mbps
Bandwith@CL=6	533	667	800	Mbps
CL-tRCD-tRP	4-4-4	5-5-5	6-6-6	tCK



Part Number Information

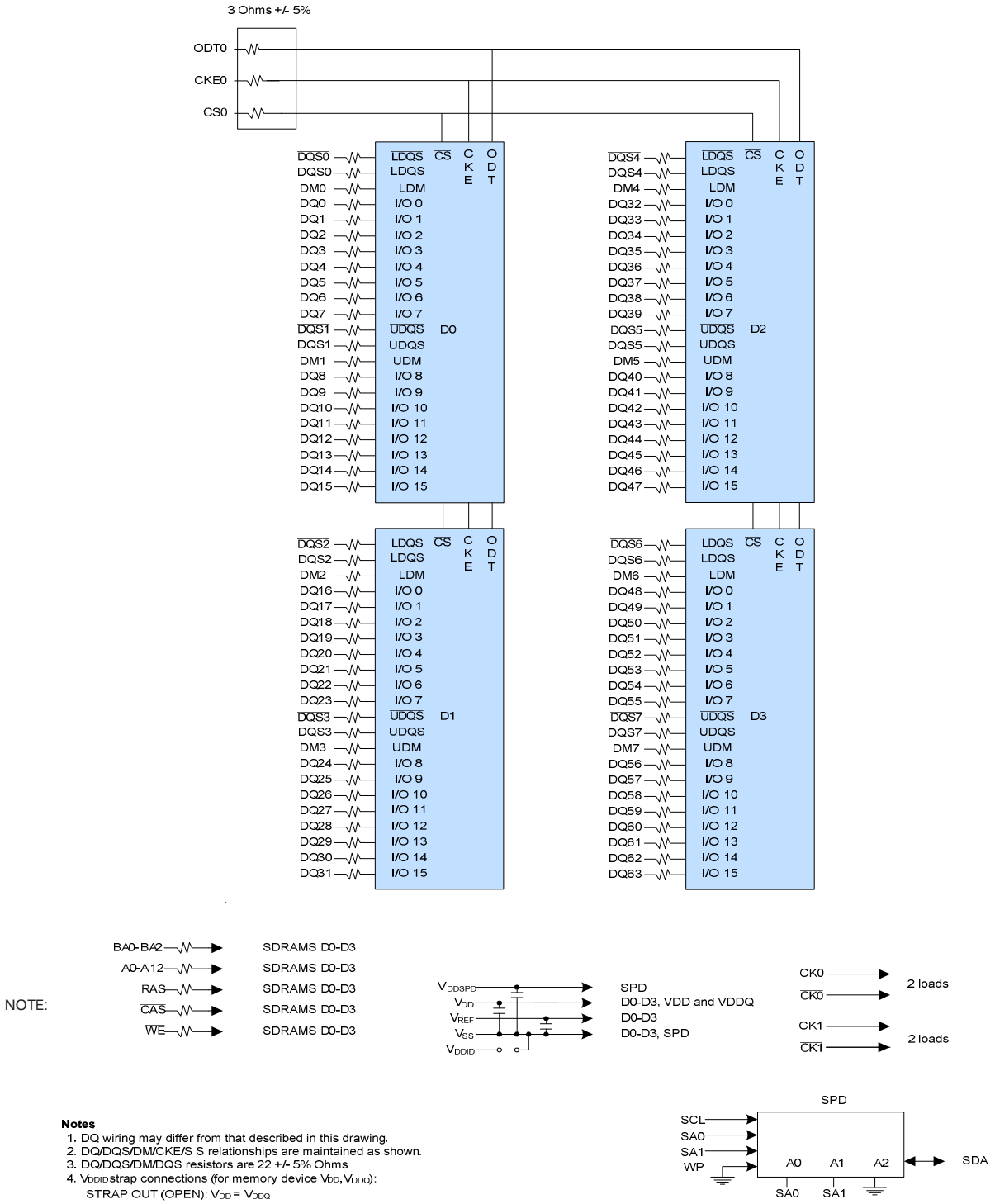


BASED ON	X4	X16	X8
240PIN DIMM UNBUFFERED	I	J	K
240PIN DIMM REGISTERED	N	O	U
200PIN SO-DIMM	V	B	G
172PIN Micro-DIMM			M

Block Diagram

Functional Block Diagram

[512MB – 1 Rank, 64Mx16 DDR2 SDRAMs]



NOTE:

Notes

1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22 +/- 5% Ohms
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$

512MB/1GB/2GB DDR2 SDRAM SODIMM Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	2	V_{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V_{SS}	4	DQ4	53	V_{SS}	54	V_{SS}	103	V_{DD}	104	V_{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V_{SS}	156	V_{SS}
7	DQ1	8	V_{SS}	57	DQ19	58	DQ23	107	BA0	108	$\overline{RAS}$	157	DQ48	158	DQ52
9	V_{SS}	10	DM0	59	V_{SS}	60	V_{SS}	109	$\overline{WE}$	110	$\overline{CS0}$	159	DQ49	160	DQ53
11	$\overline{DQS0}$	12	V_{SS}	61	DQ24	62	DQ28	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{CAS}$	114	ODT0	163	NC	164	CK1
15	V_{SS}	16	DQ7	65	V_{SS}	66	V_{SS}	115	$\overline{CS1}$/NC	116	A13/NC	165	V_{SS}	166	$\overline{CK1}$
17	DQ2	18	V_{SS}	67	DM3	68	$\overline{DQS3}$	117	V_{DD}	118	V_{DD}	167	$\overline{DQS6}$	168	V_{SS}
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1/NC	120	NC	169	DQS6	170	DM6
21	V_{SS}	22	DQ13	71	V_{SS}	72	V_{SS}	121	V_{SS}	122	V_{SS}	171	V_{SS}	172	V_{SS}
23	DQ8	24	V_{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	V_{SS}	78	V_{SS}	127	V_{SS}	128	V_{SS}	177	V_{SS}	178	V_{SS}
29	$\overline{DQS1}$	30	CK0	79	CKE0	80	CKE1/NC	129	$\overline{DQS4}$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK0}$	81	V_{DD}	82	V_{DD}	131	DQS4	132	V_{SS}	181	DQ57	182	DQ61
33	V_{SS}	34	V_{SS}	83	NC	84	NC	133	V_{SS}	134	DQ38	183	V_{SS}	184	V_{SS}
35	DQ10	36	DQ14	85	BA2	86	NC	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS7}$
37	DQ11	38	DQ15	87	V_{DD}	88	V_{DD}	137	DQ35	138	V_{SS}	187	V_{SS}	188	DQS7
39	V_{SS}	40	V_{SS}	89	A12	90	A11	139	V_{SS}	140	DQ44	189	DQ58	190	V_{SS}
41	V_{SS}	42	V_{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V_{SS}	193	V_{SS}	194	DQ63
45	DQ17	46	DQ21	95	V_{DD}	96	V_{DD}	145	V_{SS}	146	$\overline{DQS5}$	195	SDA	196	V_{SS}
47	V_{SS}	48	V_{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS2}$	50	NC	99	A3	100	A2	149	V_{SS}	150	V_{SS}	199	V_{DDSPD}	200	SA1

Note: All pin assignments are consistent for all 8-byte unbuffered versions.

CKE1, $\overline{CS1}$ and ODT1 are for 1GB/2GB modules only.

A13 is for 2GB modules only.

Pin Description

Symbol	Type	Function
CK0-CK2 CK0#-CK2#	Input	CK and CK# are differential clock inputs. All the SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (read) data is reference to the crossing of CK and CK# (Both directions of crossing)
CKE0-CKE1	Input	Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clocks, CKE low initiates the Powe Down mode, or the Self-Refresh mode
S0#-S1#	Input	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disbled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks
RAS#, CAS#, WE#	Input	RAS#, CAS#, WE# (ALONG WITH CS#) define the command being entered.
ODT0-ODT1	Input	When high, termination resistance is enabled for all DQ, DQ# and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
V_{REF}	Supply	Reference voltage for SSTL 18 inputs.
V_{DDQ}	Supply	Power supply for the DDR II SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
BA0-BA1	Input	Selects which SDRAM BANK of four is activated.
A0-A13	Input	During a Bank Activate command cycle, Address input defines the row address (RA0-RA13) During a Read or Write command cycle, Address input defines the colum address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disbled. During a precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1. If AP is low, BA0, BA1are used to define which bank to precharge.
DQ0-DQ63 CB0-CB7	In/Out	Data and Check Bit Input/Output pins.
DM0-DM8	Input	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply	Power and ground for DDR2 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS0-DQS8 DQS0#-DQS8#	In/Out	Data strobe for input and output data. its edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SA0-SA2	Input	These signals and tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EERPOM address range.
SDA	In/Out	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pullup onthe system board.
V_{DD} SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 1.7V to 3.6V.

Serial Presence Detect Information

Bin Sort:

E4 (PC2-4200 @ CL4) F5 (PC2-5300 @ CL5) G6 (PC2-6400 @ CL6)

Byte #	Function described	Function Supported			Hex value		
		E4	F5	G6	E4	F5	G6
0	Defines # of Bytes written into serial memory at module manufacturer	128bytes			80h		
1	Total # of Bytes of SPD memory device	256bytes			08h		
2	Fundamental memory type	SDRAM DDR2			08h		
3	# of row address on this assembly	13			0Dh		
4	# of column address on this assembly	10			0Ah		
5	Module attributes-Number of DIMM Ranks, Package and Height	1.18in., singel rank			60h		
6	Data width of this assembly	64 bits			40h		
7	.....Data width of this assembly	-			00h		
8	VDDQ and interface standard of this assembly	SSTL 1.8V			05h		
9	DDR SDRAM cycle time at CL=X	3.75ns	3.0ns	2.5ns	3Dh	30h	25h
10	DDR SDRAM Access time from clock at CL=X	±0.50ns	±0.45ns	±0.40ns	50h	45h	40h
11	DIMM configuration type(Non-parity, Parity, ECC)	Unbuffered			00h		
12	Refresh rate & type	7.8us & Self refresh			82h		
13	Primary DDR SDRAM width	x16			10h		
14	Error checking DDR SDRAM data width	N/A			00h		
15	Reserved	-			00h		
16	DDR SDRAM device attributes : Burst lengths supported	4,8			0Ch		
17	DDR SDRAM device attributes : # of banks on each DDR SDRAM	8 banks			08h		
18	DDR SDRAM device attributes : CAS Latency supported	4	4,5	4,5,6	10h	30h	70h
19	DIMM Mechanical Thickness	<3.8mm			01h		
20	DDR2 DIMM Type	SODIMM			04h		
21	DDR2 SDRAM module attributes	-			00h		
22	DDR2 SDRAM device attributes : General	PASR/ODT 50ohm/Weak driver			07h		
23	DDR SDRAM cycle time at CL=X-1	-	3.75ns	3.0ns	00	3Dh	30h
24	DDR SDRAM Access time from CL=X-1	-	±0.50ns	±0.45ns	00	50h	45h
25	DDR SDRAM cycle time at CL=X-2	-		3.75ns	00		3Dh
26	DDR SDRAM Access time from CL=X-2	-		±0.50ns	00		50h
27	Minimum row precharge time (=t_{RP})	15ns	15ns	15ns	3Ch	3Ch	3Ch
28	Minimum row activate to row active delay (=t_{RRD})	10ns	10ns	10ns	28h	28h	28h
29	Minimum RAS to CAS delay (=t_{RCD})	15ns	15ns	15ns	3Ch	3Ch	3Ch
30	Minimum RAS pulse with t_{RAS}	45ns	45ns	45ns	2Dh	2Dh	2Dh

Byte #	Function described	Function Supported			Hex value		
		E4	F5	G6	E4	F5	G6
31	Module Rank density	512MB			80h		
32	Command and address signal input setup time	0.25ns	0.20ns	0.175ns	25h	20h	17h
33	Command and address signal input hold time	0.37ns	0.27ns	0.25ns	37h	27h	25h
34	Data signal input setup time	0.10ns	0.05ns	0.05ns	10h	05h	05h
35	Data signal input hold time	0.22ns	0.17ns	0.125ns	22h	17h	12h
36	Write Recovery Time (=t_{WR})	15ns			3Ch		
37	Write to Read CMD delay (=t_{WTR})	7.5ns	7.5ns	7.5ns	1Eh	1Eh	1Eh
38	Read to Precharge CMD delay (=t_{RTP})	7.5ns			1Eh		
39	Mem Analysis Probe	00	00	00	00		
40	Extension for bytes 41 and 42				06H		
41	SDRAM device minimum active to active/auto-refresh time (=t_{RC})	60ns	60ns	60ns	3Ch	3Ch	3Ch
42	SDRAM device minimum active to autorefresh to active/auto-refresh time (=t_{RFC})	127.5ns			7Fh		
43	SDRAM device maximum device cycle time (=$t_{CK\ MAX}$)	8ns			80h		
44	SDRAM device maximum skew between DQS and DQ signals (=t_{DQSQ})	0.30ns	0.24ns	0.20ns	1Eh	18h	14h
45	SDRAM device maximum read datahold skew factor (=t_{QHS})	0.40ns	0.34ns	0.30ns	28h	22h	1Eh
46	PLL Relock Time	-			00h		
47	Tcase max , DT4R4W	00	00	00	00h	00h	00h
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient	00	00	00	00h	00h	00h
49	DRAM case Temperature Rise from Ambient due to Active Precharge / Mode Bits (DT0/Mode Bits)	00	00	00	00h	00h	00h
50	DRAM case Temperature Rise from Ambient due to Precharge / Quiet Standy (DT2N/DT2O)	00	00	00	00h	00h	00h
51	DRAM case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)	00	00	00	00h	00h	00h
52	DRAM case Temperature Rise from Ambient due to Active Standy (DT3N)	00	00	00	00h	00h	00h
53	DRAM case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	00	00	00	00h	00h	00h
54	DRAM case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	00	00	00	00h	00h	00h
55	DRAM case Temperature Rise from Ambient due to Page Open Burst Read / DT4R4W Mode bit (DT4R/DT4R4W)	00	00	00	00h	00h	00h
56	DRAM case Temperature Rise from Ambient due to Burst Refresh (DT5B)	00	00	00	00h	00h	00h

Byte #	Function described	Function Supported			Hex value		
		E4	F5	G6	E4	F5	G6
57	DRAM case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	00	00	00	00h	00h	00h
58 - 61	Superset information (may be used in future)	-			00h		
62	SPD data revision code	1.3			13h		
63	Checksum for Bytes 0 ~ 62	-			88h	E6h	73h
64	Manufacturer JEDEC ID code	DELSON			40h		
65 - 71	..... Manufacturer JEDEC ID code				00h		
72	Manufacturing location	02=Taiwan 05=China 0A=S-CH 04=Malaysia					
73 - 90	Module part number (ASCII)	D916764B24QC					
91	Manufacturer revison code (For PCB)	0			00		
92	Manufacturer revison code (For component)	0			00		
93	Manufacturing date (Year) in BCD. Example: Year 2006 = 06h	-			-		
94	Manufacturing date (Week) in BCD. Example: Week 28 = 28h	-			-		
95~98	Assembly serial #	-			-		
99~127	Manufacturer specific data (may be used in future)	Undefined			00h		
128~255	Open for customer use	Undefined			00h		

Absolute Maximum DC Ratings

Parameter	Symbol	MIN	MAX	UNITS
VDD Supply Voltage relative to VSS	VDD	-1.0	2.3	V
VDDQ Supply Voltage relative to VSS	VDDQ	-0.5	2.3	V
VDDL Supply Voltage relative to VSS	VDDL	-0.5	2.3	V
Voltage on any pin relative to VSS	VIN, VOUT	-0.5	2.3	V
Storage Temperature	T_{STG}	-55	100	^{o}C

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device.

AC & DC Operating Conditions
Recommended DC Operating Conditions

Parameter	Symbol	MIN	NOM	MAX	UNITS	Notes
VDD Supply Voltage relative to VSS	VDD	1.7	1.8	1.9	V	1
VDDQ Supply Voltage relative to VSS	VDDQ	1.7	1.8	1.9	V	4
VDDL Supply Voltage relative to VSS	VDDL	1.7	1.8	1.9	V	4
I/O Reference Voltage	VREF	0.49xVDDQ	0.50xVDDQ	0.51xVDDQ	V	2
I/O Termination Voltage(system)	VTT	VREF-0.04	VREF	VREF+0.04	V	3

Note:
1. VDD and VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal to VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak to Peak AC noise on the VREF may not exceed +/-2% VREF(DC).
3. VTT of the transmitting device must track VREF of receiving device.
4. VDDQ tracks with VDD; VDDL tracks with VDD.

Input Electrical Characteristics and operating Conditions

Input DC Logic Levels

Parameter	Symbol	MIN	MAX	UNITS
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.125	VDDQ+0.3	V
Input Low (Logic 0) Voltage	VIL(DC)	-0.3	VREF-0.125	V

Input AC Logic Levels

Parameter	Symbol	DDR2 533		DDR2 667, 800		
		MIN	MAX	MIN	MAX	UNITS
ac input logic high	VIH(AC)	VREF+0.250	-	VREF+0.20	-	V
ac input logic low	VIL(AC)	-	VREF-0.250	-	VREF-0.20	V

DDR2 IDD Current Definitions

Symbol	Proposed Conditions		Units	Notes
IDD0	**Operating one bank active-precharge current**; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC (IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address businputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputsare STABLE; Data bus inputs are FLOATING		mA	
IDD2N	**Precharge standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD3P	**Active power-down current**; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	mA	
		Slow PDN Exit MRS(12) = 1mA	mA	
IDD3N	**Active standby current**; All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD5B	**Burst auto refresh current**; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD6	**Self refresh current**; CK and CK\ at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA	
		Low Power	mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, $t_{RCD} = 1*t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		mA	

DDR2 IDD Current Table

Symbol		E4 PC2-4200@CL4	F5 PC2-5300@CL5	G5 PC2-6400@CL5	G6 PC2-6400@CL6	Unit
IDD0		560	600	640	720	mA
IDD1		600	640	680	760	mA
IDD2P		64	64	64	64	mA
IDD2Q		240	240	320	320	mA
IDD2N		240	320	320	400	mA
IDD3P	Fast PDN Exit MR[12]=0	240	240	240	280	mA
	Slow PDN Exit MR[12]=1	96	96	96	96	mA
IDD3N		320	400	400	480	mA
IDD4R		600	800	880	1040	mA
IDD4W		680	880	1000	1200	mA
IDD5B		760	800	840	900	mA
IDD6	Normal	64	64	64	64	mA
	Low Power	32	32	32	32	mA
IDD7		1440	1480	1480	1600	mA

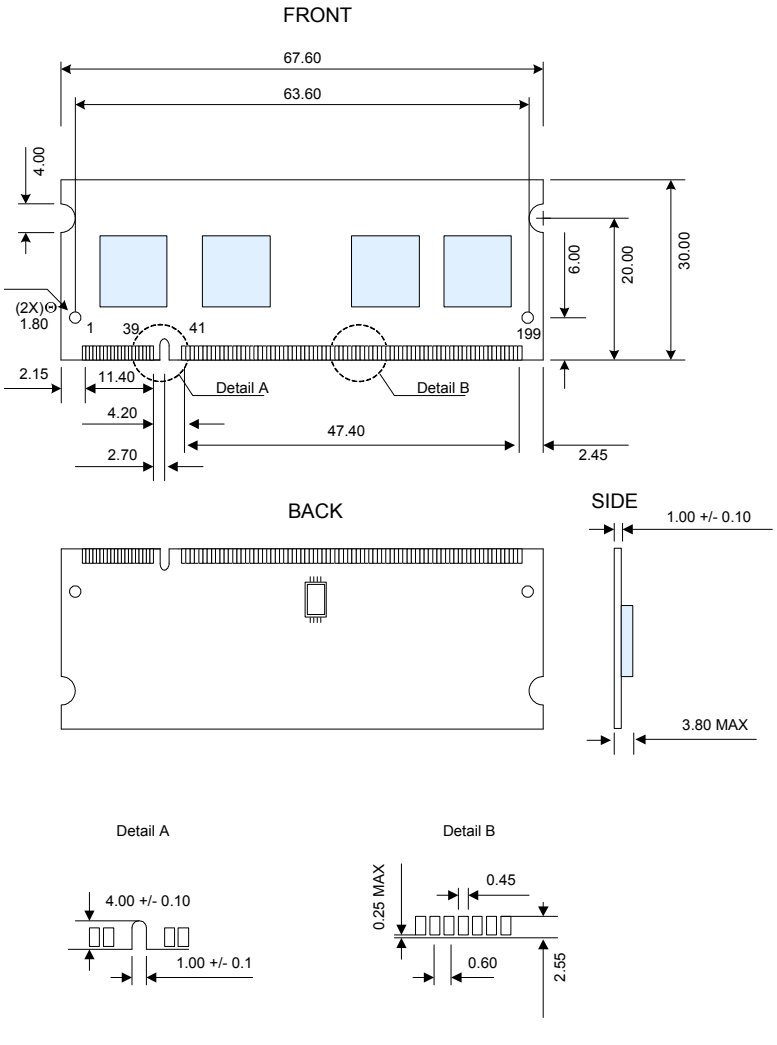
AC Characteristics (AC operating conditions unless otherwise noted)

Parameter		Symbol	(DDR2-533) -E4		(DDR2-667) -F5		(DDR2-800) -G5		(DDR2-800) -G6		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Row Cycle Time		t_{RC}	60	-	60	-	57.25	-	60	-	ns
Auto Refresh Row Cycle Time		t_{RFC}	105	-	105	-	105	-	105	-	ns
Row Active Time		t_{RAS}	45	70K	45	70K	45	70K	45	70K	ns
Row Address to Column Address Delay		t_{RCD}	15	-	15	-	12.5	-	15	-	ns
Row Active to Row Active Delay (x4 & x8)		t_{RRD}	7.5	-	7.5	-	7.5	-	7.5	-	ns
Row Active to Row Active Delay (x16)		t_{RRD}	10	-	10	-	10	-	10	-	ns
Column Address to Column Address Delay		t_{CCD}	2	-	2	-	2	-	2	-	CLK
Row Precharge Time		t_{RP}	15	-	15	-	12.5	-	15	-	ns
Write Recovery Time		t_{WR}	15	-	15	-	15	-	15	-	ns
Last Data-In to Read Command		t_{DRL}	1	-	1	-	1	-	1	-	CLK
Auto Precharge Write Recovery + Precharge Time		t_{DAL}	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	ns
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	t_{CK}	5	8	5	8	5	8	-	-	ns
	$\overline{CAS}$ Latency = 4		3.75	8	3.75	8	3.75	8	3.75	8	ns
	$\overline{CAS}$ Latency = 5		3.75	8	3	8	2.5	8	3	8	ns
	$\overline{CAS}$ Latency = 6		-	-	-	-	-	-	2.5	8	ns
Clock High Level Width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CLK
Clock Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CLK
Data-Out edge to Clock edge Skew		t_{AC}	-0.50	0.50	-0.45	0.45	-0.40	0.40	-0.40	0.40	ns
DQS-Out edge to Clock edge Skew		t_{DQSCK}	-0.45	0.45	-0.40	0.40	-0.35	0.35	-0.35	0.35	ns
DQS-Out edge to Data-Out edge Skew		t_{DQSQ}	-	0.30	-	0.24	-	0.20	-	0.20	ns
Data-Out hold time from DQS		t_{QH}	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	ns
Data hold skew factor		t_{QHS}	-	400	-	340	-	300	-	300	ps
Clock Half Period		t_{HP}	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	ns
Input Setup Time (fast slew rate)		t_{IS}	250	-	200	-	175	-	175	-	ps
Input Hold Time (fast slew rate)		t_{IH}	375	-	275	-	250	-	250	-	ps
Input Pulse Width		t_{IPW}	0.60	-	0.60	-	0.60	-	0.60	-	CLK
Write DQS High Level Width		t_{DQSH}	0.35		0.35		0.35		0.35		CLK
Write DQS Low Level Width		t_{DQSL}	0.35		0.35		0.35		0.35		CLK
CLK to First Rising edge of DQS-In		t_{DQSS}	WL-$0.25t_{CK}$	WL+$0.25t_{CK}$	WL-$0.25t_{CK}$	WL+$0.25t_{CK}$	WL-$0.25t_{CK}$	WL+$0.25t_{CK}$	WL-$0.25t_{CK}$	WL+$0.25t_{CK}$	CLK
Data-In Setup Time to DQS-In (DQ & DM)		t_{DS}	100	-	50	-	50	-	50	-	ps
Data-in Hold Time to DQS-In (DQ & DM)		t_{DH}	225	-	175	-	125	-	125	-	ps

Parameter	Symbol	(DDR2-533) -E4		(DDR2-667) -F5		(DDR2-800) -G5		(DDR2-800) -G6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
DQS falling edge to CLK rising Setup Time	t_{DSS}	0.2	-	0.2	-	0.2	-	0.2	-	CLK
DQS falling edge from CLK rising Hold Time	t_{DSH}	0.2	-	0.2	-	0.2	-	0.2	-	CLK
DQ & DM Input Pulse Width	t_{DIPW}	0.35	-	0.35	-	0.35	-	0.35	-	CLK
Read DQS Preamble Time	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	CLK
Read DQS Postamble Time	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK
Write DQS Preamble Setup Time	t_{WPRES}	0	-	0	-	0	-	0	-	CLK
Write DQS Preamble Hold Time	t_{WPREH}	0.25	-	0.25	-	0.25	-	0.25	-	CLK
Write DQS Postamble Time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	7.5	-	ns
Internal write to read command delay	t_{WTR}	7.5	-	7.5	-	7.5	-	7.5	-	ns
Data out high impedance time from CLK/$\overline{CLK}$	t_{HZ}	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	ns
Data out low impedance time from CLK/$\overline{CLK}$	t_{LZ}	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	ns
Mode Register Set Delay	t_{MRD}	2	-	2	-	2	-	2	-	CLK
Exit Self Refresh to Non-Read Command	t_{XSNR}	t_{RFC}+10	-	t_{RFC}+10	-	t_{RFC}+10	-	t_{RFC}+10	-	ns
Exit Self Refresh to Read Command	t_{XSRD}	200	-	200	-	200	-	200	-	CLK
Exit Precharge Power Down to any non-Read Command	t_{XP}	2	-	2	-	2	-	2	-	CLK
Exit Active Power Down to Read Command	t_{XARD}	2	-	2	-	2	-	2	-	CLK
Exit Active Power Down to Read Command (Slow exit, Lower Power)	t_{XARDS}	6-AL	-	6-AL	-	6-AL	-	6-AL	-	CLK
ODT drive mode output delay	t_{OIT}	0	12	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	t_{Delay}	tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		ns
CKE minimum high and low pulse width	t_{CKE}	3	-	3	-	3	-	3	-	CLK

Package Dimensions

[512MB – 1 Rank, 64Mx16 DDR2 SDRAMs]



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.
Units: Millimeters (Inches)

Note: Device position and scale are only for reference.

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