8Gb NAND Flash

Single-Level-Cell (1bit/cell)

Rev.1.1 Sept. 2018

1.0 INTRODUCTION

1.1 General Description

Offered in 1Gx8bit, the DNS8G08U0F is a 8G-bit NAND Flash Memory with spare 128M-bit. The device is offered in 3.3V V_{CC}. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 400 μs on the (2K+64)Byte page and an erase operation can be performed in typical 4.5ms on a (128K+4K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The DNS8G08U0F is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

1.2 Features

FEATURES

xVoltage Supply
- 2.70V ~ 3.60V

xOrganization
- Memory Cell Array : (1G + 32M) x 8bit
- Data Register : (2K + 64) x 8bit

xAutomatic Program and Erase
- Page Program : (2K + 64)Byte
- Block Erase : (128K + 4K)Byte

xPage Read Operation
- Page Size : (2K + 64)Byte
- Random Read : 20 μs(Max.)
- Serial Access : 25ns(Min.)
* K9NBG08U5M : 50ns(Min.)

xFast Write Cycle Time
- Page Program time : 200 μs(Typ.)
- Block Erase Time : 1.5ms(Typ.)

xCommand/Address/Data Multiplexed I/O Port

xHardware Data Protection
- Program/Erase Lockout During Power Transitions

xReliable CMOS Floating-Gate Technology
- Endurance : 100K Program/Erase Cycles (with 1bit/512Byte ECC)
- Data Retention : 10 Years

xCommand Driven Operation

xIntelligent Copy-Back with internal 1bit/528Byte EDC

xUnique ID for Copyright Protection

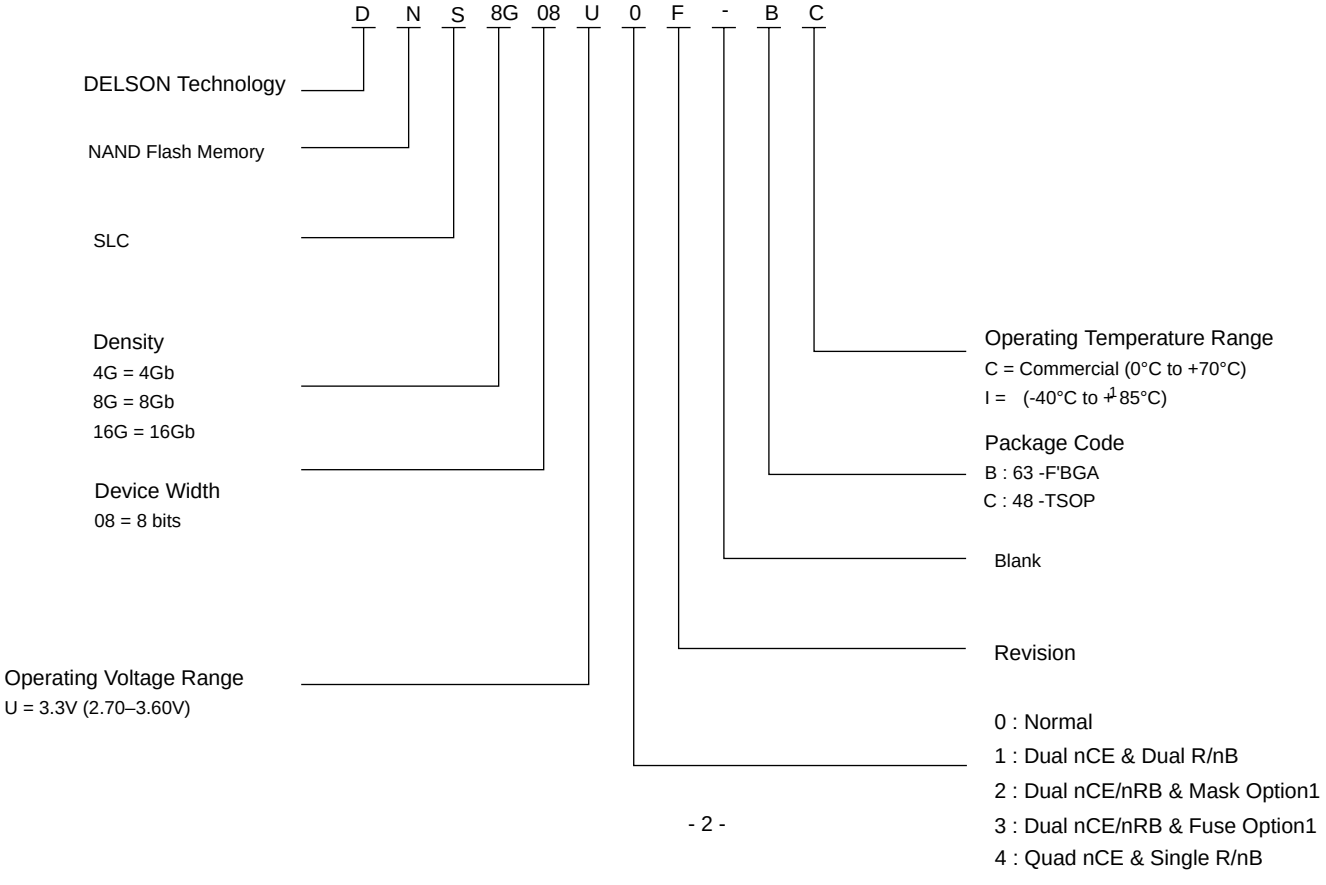
xPackage :
- DNS8G08U0F-BC Pb-Free, Halogen-Free Package
63 - FBGA (9 x 11 / 0.8 mm pitch)

1.3 Product List

Part Number	Density	Organization	V_{CC} Range	PKG Type
DNS4G08U0F-BC	4Gb	x8	2.7V ~ 3.6V	TSOP
DNS8G08U0F-BC	8Gb			

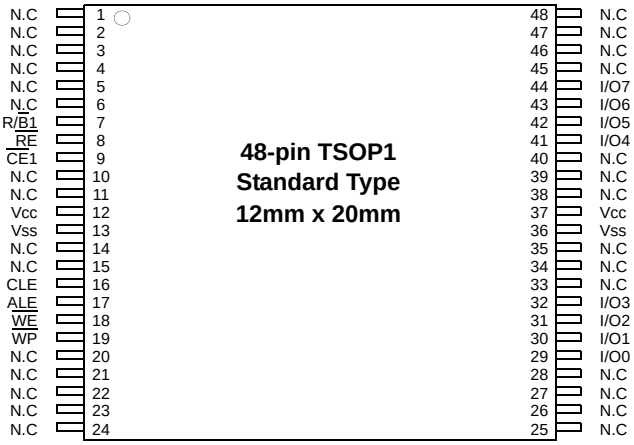
Part Number	Density	Organization	V_{CC} Range	PKG Type
DNS4G08U0F-BC	4Gb	x8	2.7V ~ 3.6V	63 FBGA
DNS8G08U0F-BC	8Gb			

Part Number Chart



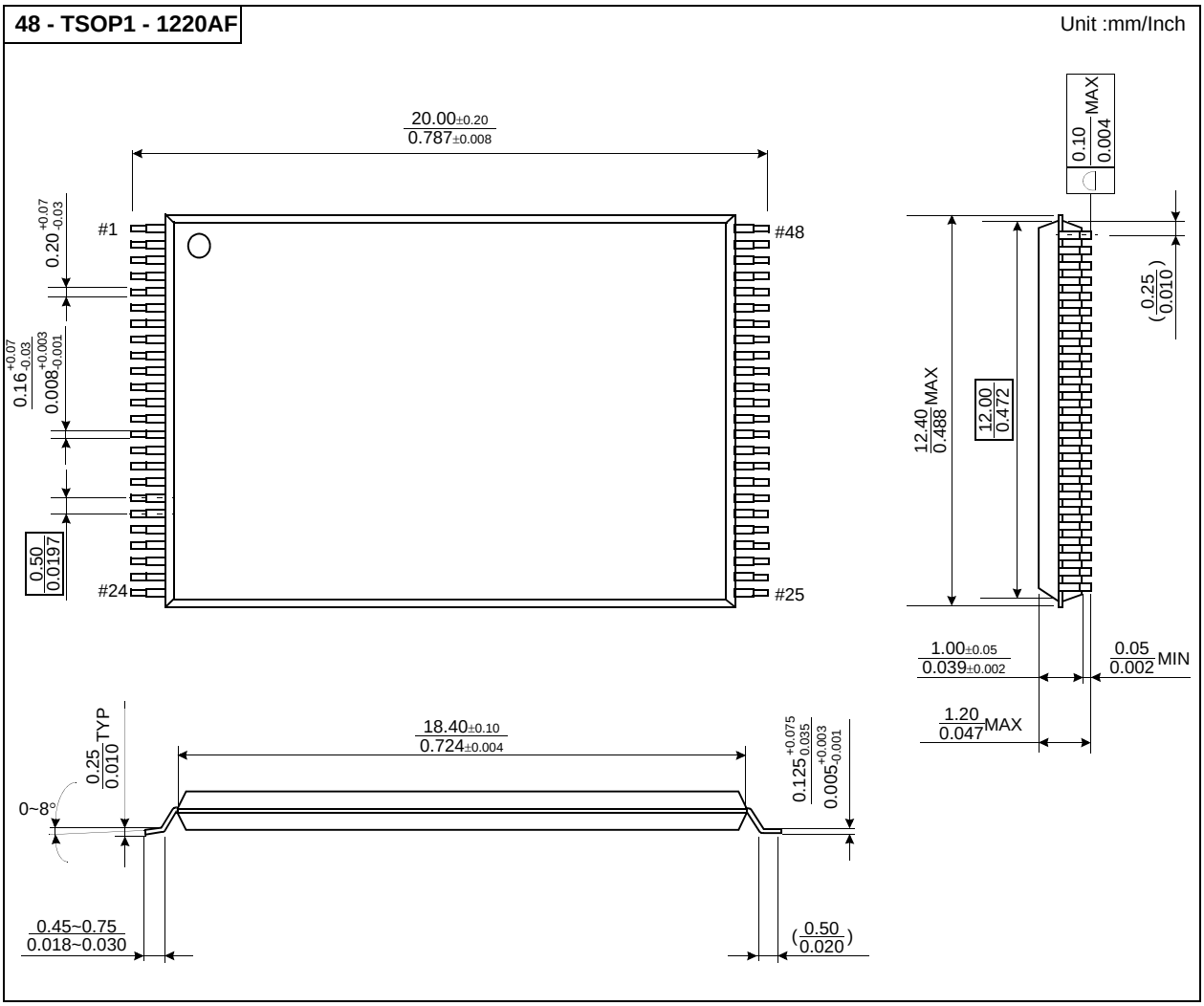
1.4 Pin Configuration (TSOP1)

DNS8G08U0F-CC
DNS8G08U0F-CC



1.4.1 Package Dimensions

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



1.5 Pin Configuration (FBGA)

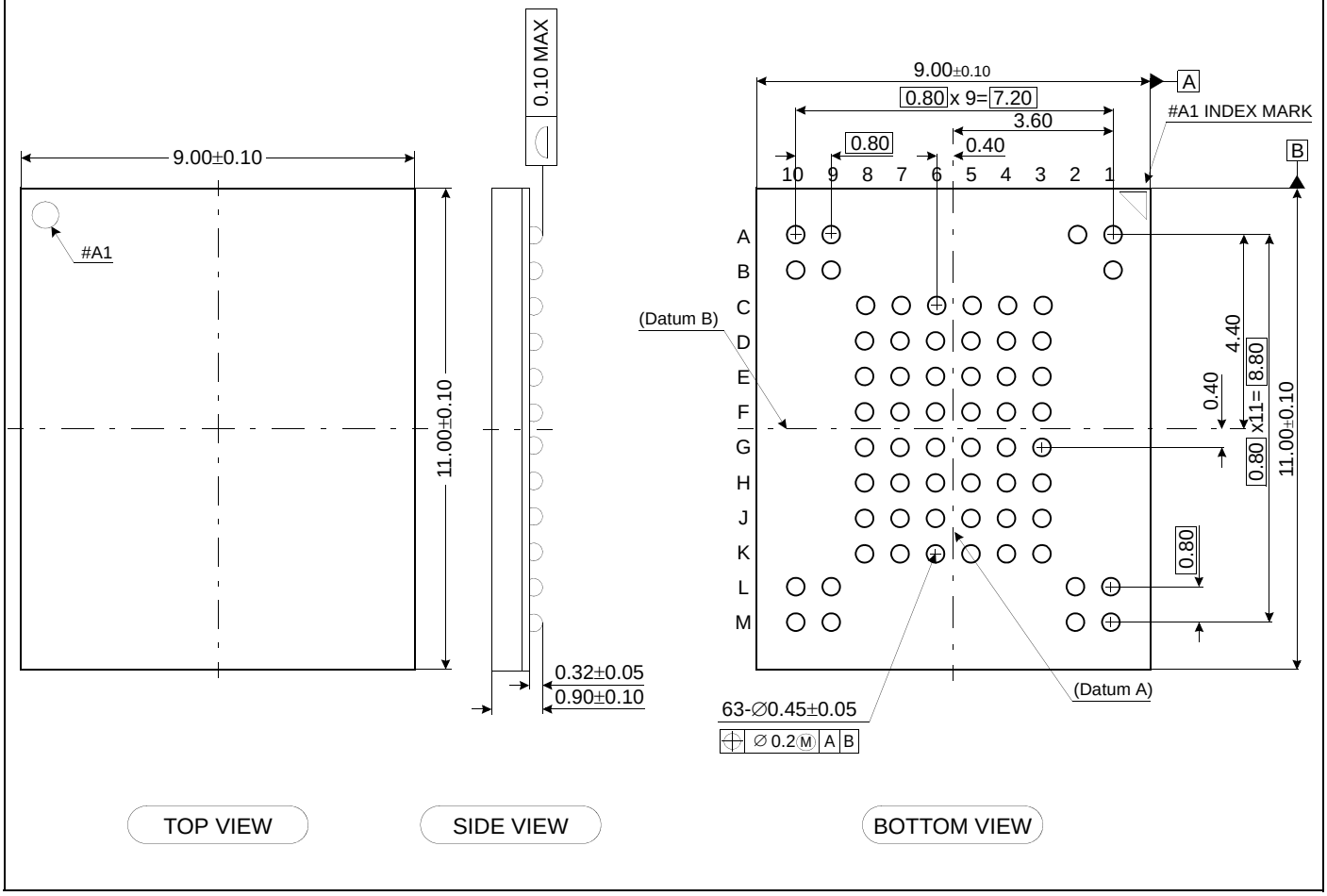
DNS8G08U0F-BC

Top View

	1	2	3	4	5	6	7	8	9	10
A	N.C	N.C							N.C	N.C
B	N.C								N.C	N.C
C			/WP	ALE	Vss	/CE	/WE	R/B		
D			NC	/RE	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	NC	NC		
G			NC	NC	NC	NC	NC	NC		
H			NC	I/O0	NC	NC	NC	Vcc		
J			NC	I/O1	NC	Vcc	I/O5	I/O7		
K			Vss	I/O2	I/O3	I/O4	I/O6	Vss		
L	N.C	N.C							N.C	N.C
M	N.C	N.C							N.C	N.C

1.6 Package Dimensions

63-Ball FBGA (measured in millimeters)



1.7 Pin Descriptions

[Table 1] Pin Descriptions

Pin Name	Pin Function
I/O_0 ~ I/O_7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
V_{CC}	**POWER** V_{CC} is the power supply for device.
V_{SS}	**GROUND**
N/C	**NO CONNECTION**

NOTE :
Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC} or V_{SS} disconnected.

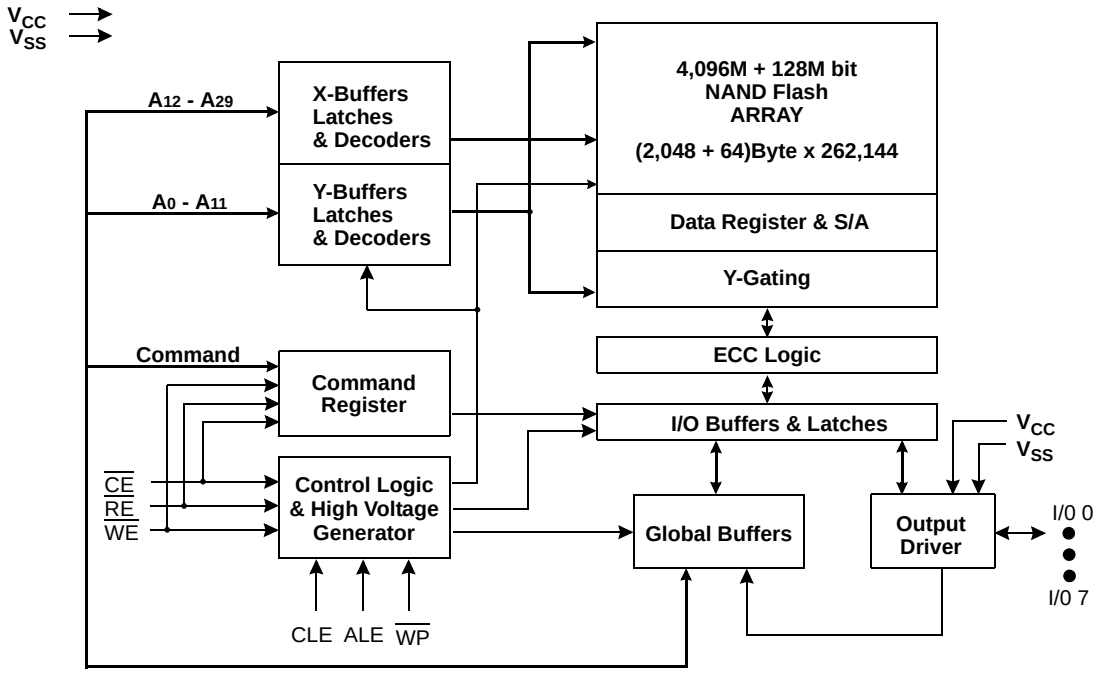


Figure 1.D9F4G08U0F Functional Block Diagram

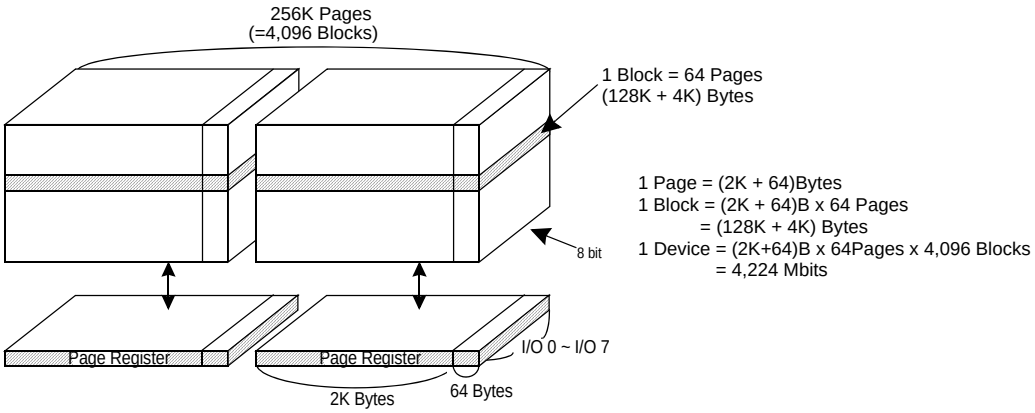


Figure 2. D9F4G08U0F Array Organization

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Column Address
2nd Cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	
3rd Cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	Row Address :
4th Cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	Page Address : A_{12} ~ A_{17} Plane Address : A_{18}
5th Cycle	A_{28}	A_{29}	**A_{30}	*L	*L	*L	*L	*L	Block Address : A_{19} ~ A_{29}

NOTE :

Column Address : Starting Address of the Register.

* L must be set to "Low".
* The device ignores any additional input of address cycles than required.

**A_{30} is used for DDP with a single $\overline{CE}$.

**A_{30} must be set to "Low" for SDP.

2.0 PRODUCT INTRODUCTION

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Read Status Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The 528M byte physical space requires 30 addresses, thereby requiring five cycles for addressing : 2 cycles of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 2 defines the specific commands of the DNS4G08U0F/DNS8G08U0F.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

[Table 2] Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Two-Plane Page Program[2)]	80h---11h	81h---10h	
Copy-Back Program	85h	10h	
Two-Plane Copy-Back Program[2)]	85h---11h	81h---10h	
Block Erase	60h	D0h	
Two-Plane Block Erase	60h---60h	D0h	
Random Data Input[1)]	85h	-	
Random Data Output[1)]	05h	E0h	
Read Status	70h		O
ECC Read Status	7Ah		
Chip1 Status[3)]	F1h		O
Chip2 Status[3)]	F2h		O

NOTE :

1) Random Data Input/Output can be executed in a page.

2) Any command between 11h and 81h is prohibited except 70h and FFh.

3) Interleave-operation between two chips is allowed.
It's prohibited to use F1h and F2h commands for other operations except interleave-operation.

Caution :

Any undefined command inputs are prohibited except for above command set of Table 2.

2.1 Valid Block

[Table 3] The Number of Valid Block per a $\overline{CE}$

Parameter	Symbol	Min	Typ.	Max	Unit
DNS4G08U0F	N_{VB}	4,016	-	4,096	Blocks
DNS8G08U0F		8,032		8,192	

NOTE :
1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2) The number of valid block is on the basis of single plane operations, and this may be decreased with two plane operations.

2.2 Absolute Maximum DC Ratings

[Table 4] Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{CC}	-0.6 to +4.6	V
		V_{IN}	-0.6 to +4.6	
		$V_{I/O}$	-0.6 to Vcc + 0.3 (< 4.6V)	
Temperature Under Bias	DNS4G08U0F-BC	T_{BIAS}	-10 to +125	°C
	DNS8G08U0F-BC		-40 to +125	
Storage Temperature		T_{STG}	-65 to +150	°C
Short Circuit Current		I_{OS}	5	mA

NOTE :
1) Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2) Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.3 Recommended Operating Conditions

[Table 5] Recommended Operating Conditions

Parameter	Symbol	K9F4G08U0F			Unit
		Min	Typ.	Max	
Power Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Ground Supply Voltage	V_{SS}	0	0	0	V

2.4 DC Operating Characteristics

[Table 6] DC & Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Access Operation Current	$I_{CC}1$	tRC=50ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	15	30	mA
Program Operation Current	$I_{CC}2$	-	-	15	30	
Erase Operation Current	$I_{CC}3$	-	-	15	30	
Stand-by Current (TTL)	$I_{SB}1$	$\overline{CE}$=V_{IH}, $\overline{WP}$=$\overline{PRE}$=0V/V_{CC}	-	-	1	
Stand-by Current (CMOS)	$I_{SB}2$	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=$\overline{PRE}$=0V/V_{CC}	-	10	70	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}(max)	-	-	±10	
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}(max)	-	-	±10	
Input High Voltage	V_{IH}1)	-	0.8 x V_{CC}	-	V_{CC} + 0.3	V
Input Low Voltage, All inputs	V_{IL}1)	-	-0.3	-	0.2 x V_{CC}	
Output High Voltage Level	V_{OH}	DNS8G08U0F:I_{OH}=-400μA	2.4	-	-	
Output Low Voltage Level	V_{OL}	DNS8G08U0F:I_{OL}=2.1mA	-	-	0.4	
Output Low Current (R/$\overline{B}$)	I_{OL}(R/$\overline{B}$)	DNS8G08U0F:V_{OL}=0.4V	8	10	-	mA

NOTE :
1) V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC} + 0.4V for durations of 20ns or less.
2) Typical value is measured at V_{CC}=3.3V, T_A=25°C. Not 100% tested.
3) Table 6 applies to only one chip.

2.5 Input / Output Capacitance (T_A=25°C, V_{CC}=3.3V, f=1.0Mhz)

[Table 7] Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	8	pF
	$C_{I/O}$(W)2)	V_{IL}=0V	-	5	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	pF
	C_{IN}(W)2)	V_{IN}=0V	-	5	pF

NOTE :
1) Capacitance is periodically sampled and not 100% tested.
2) $C_{I/O}$(W)* and C_{IN}(W)* are tested at wafer level.

2.6 AC Test Condition

[Table 8] AC Test Condition

Parameter	DNS8G08U0F
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC}/2
Output Load	1 TTL GATE and C_L=50pF

2.7 Read / Program / Erase Characteristics

[Table 9] NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	t_R	-	-	25	μs
Program Time	t_{PROG}	-	400	900	μs
Dummy Busy Time for Two-Plane Page Program	t_{DBSY}	-	0.5	1	μs
Number of Partial Program Cycles	Nop	-	-	4	cycles
Block Erase Time	t_{BERS}	-	4.5	16	ms

NOTE :
1) Typical value is measured at Vcc=3.3V, T_A=25°C. Not 100% tested.
2) Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25°C temperature.

2.8 AC Timing Parameters Table

[Table 10] AC Timing Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t_{CLS}[1)]	12	-	ns
CLE Hold Time	t_{CLH}	5	-	ns
$\overline{CE}$ Setup Time	t_{CS}[1)]	20	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	12	-	ns
ALE Setup Time	t_{ALS}[1)]	12	-	ns
ALE Hold Time	t_{ALH}	5	-	ns
Data Setup Time	t_{DS}[1)]	12	-	ns
Data Hold Time	t_{DH}	5	-	ns
Write Cycle Time	t_{WC}	25	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	10	-	ns
Address to Data Loading Time	t_{ADL}[2)]	70	-	ns
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	12	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	25	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	20	ns
$\overline{CE}$ Access Time	t_{CEA}	-	25	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	30	ns
$\overline{CE}$ High to ALE, CLE or $\overline{WE}$ Don't Care	t_{CSD}	0	-	ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15	-	ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5	-	ns
Data Hold Time after $\overline{CE}$ Disable	t_{COH}	15	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	10	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	5/10/500[3)]	μs

NOTE :
1) The transition of the corresponding control pins must occur only once while $\overline{WE}$ is held low.
2) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
3) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5μs.

3.0 NAND FLASH TECHNICAL NOTES

3.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Delson. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/528Byte ECC.

3.2 Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original initial invalid block information is prohibited.

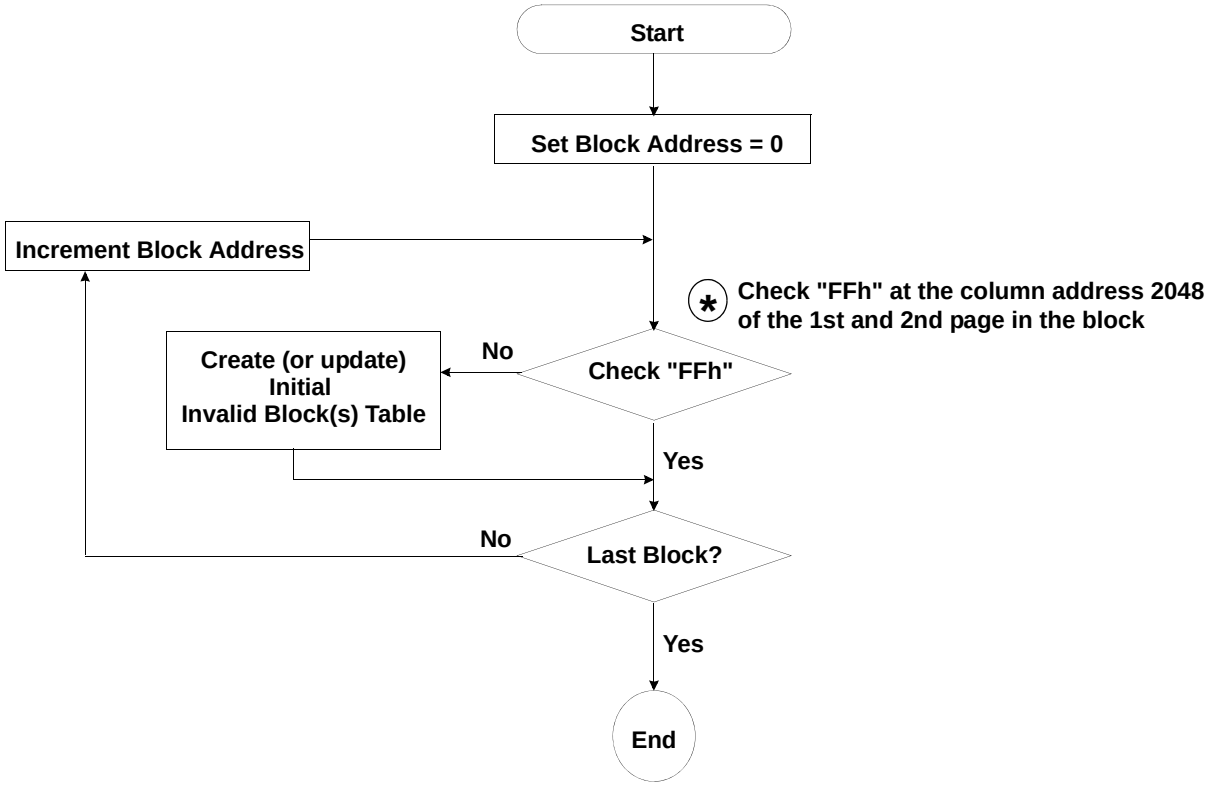


Figure 3. Flow Chart to Create Initial Invalid Block Table

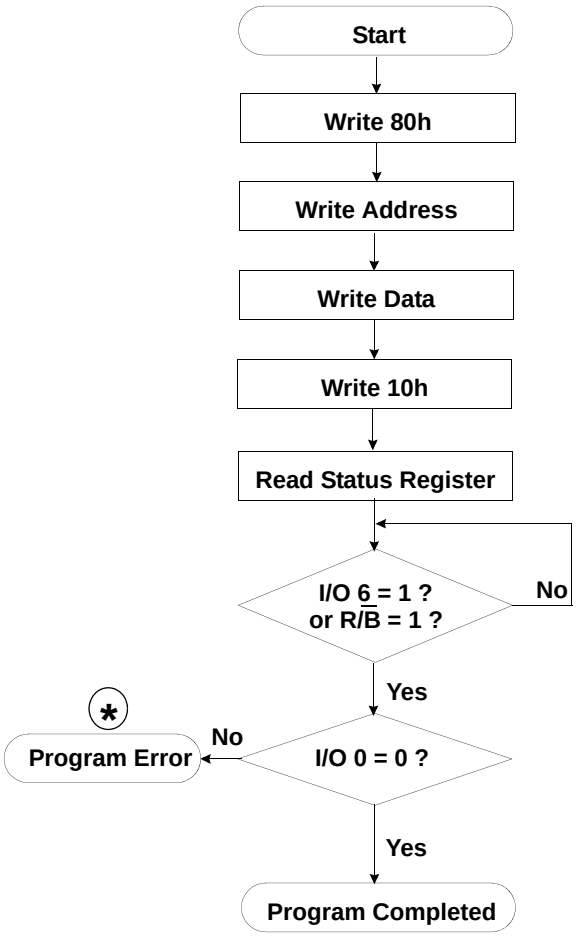
3.3 Error in Write or Read Operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of Read Status failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

[Table 11] Failure Cases

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

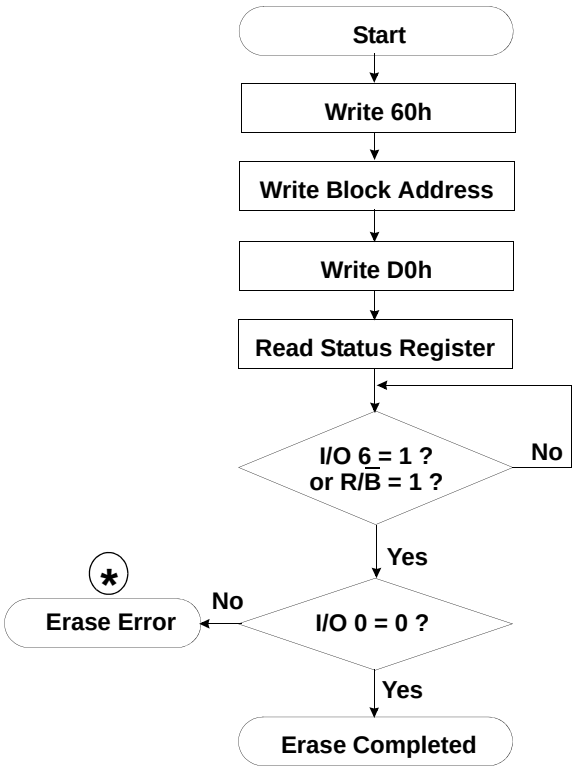
ECC : Error Correcting Code



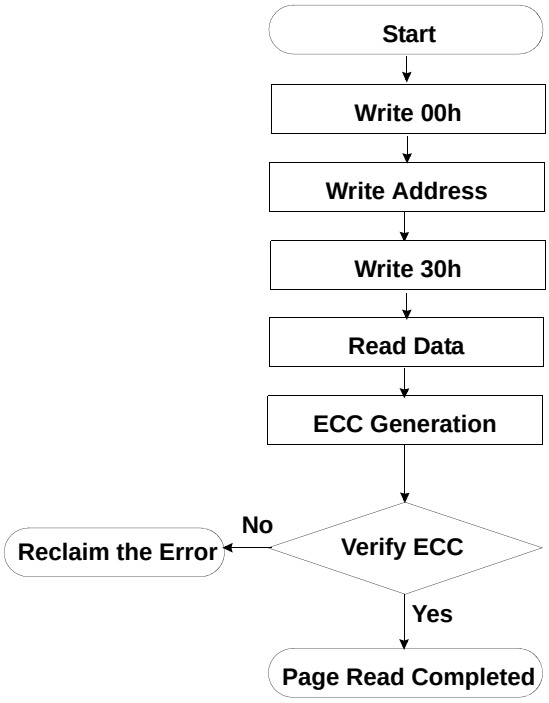
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

Figure 4. Program Flow Chart

Erase Flow Chart

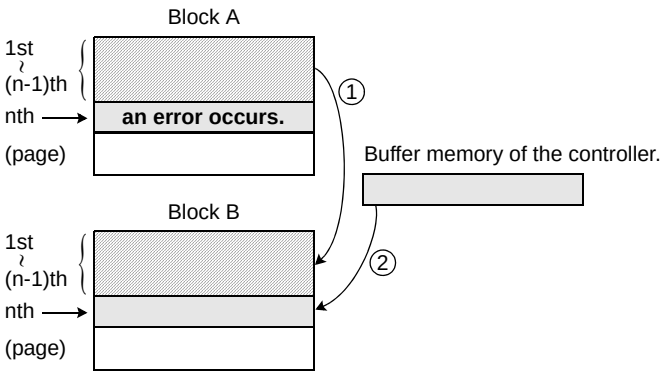


Read Flow Chart



(*) : **If erase operation results in an error, map out the failing block and replace it with another block.**

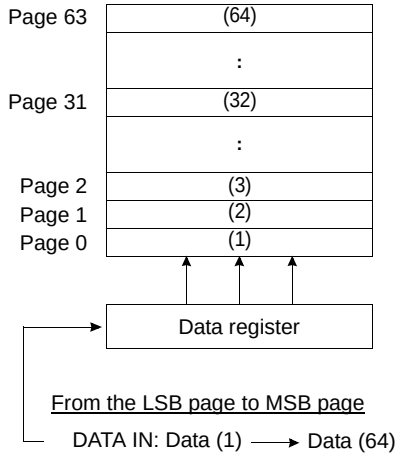
Block Replacement

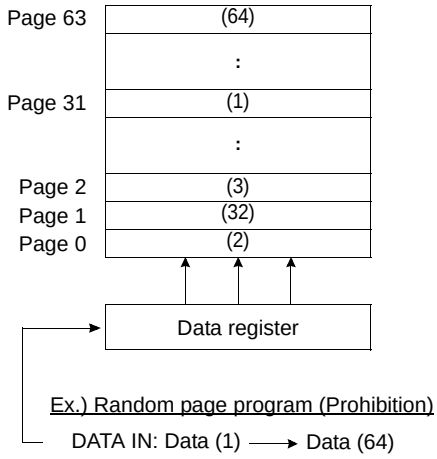


* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

3.4 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB(least significant bit) page of the block to MSB(most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.





[Table 12] Address Information

Device	DQ	DATA	ADDRESS				
	DQx	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
DNS4G08U0F	DQ 0 ~ DQ 7	2,112 Byte	A0~A7	A8~A11	A12~A19	A20~A27	A28~A29
DNS8G08U0F	DQ 0 ~ DQ 7	2,112 Byte	A0~A7	A8~A11	A12~A19	A20~A27	A28~A29

3.5 System Interface Using $\overline{CE}$ Don't-Care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or serial access as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time in the order of μ-seconds, de-activating $\overline{CE}$ during the data-loading and serial access would provide significant savings in power consumption.

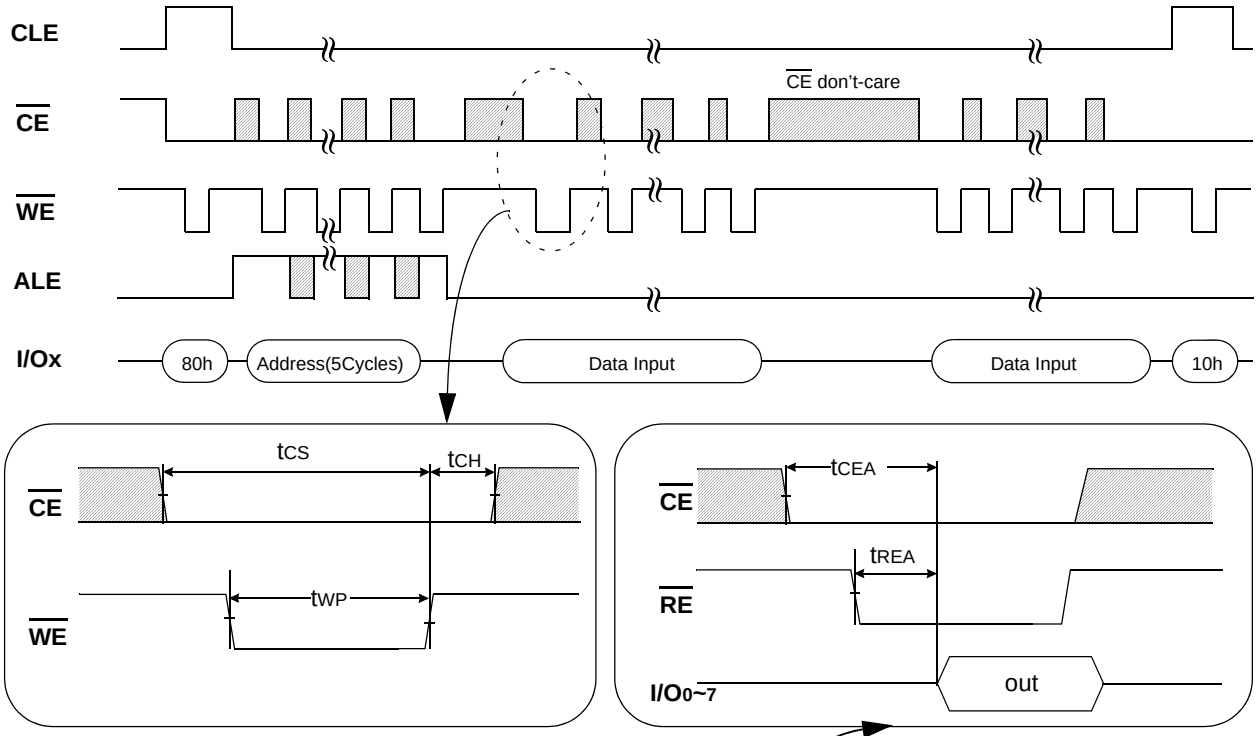


Figure 5. Program Operation with $\overline{CE}$ don't-care

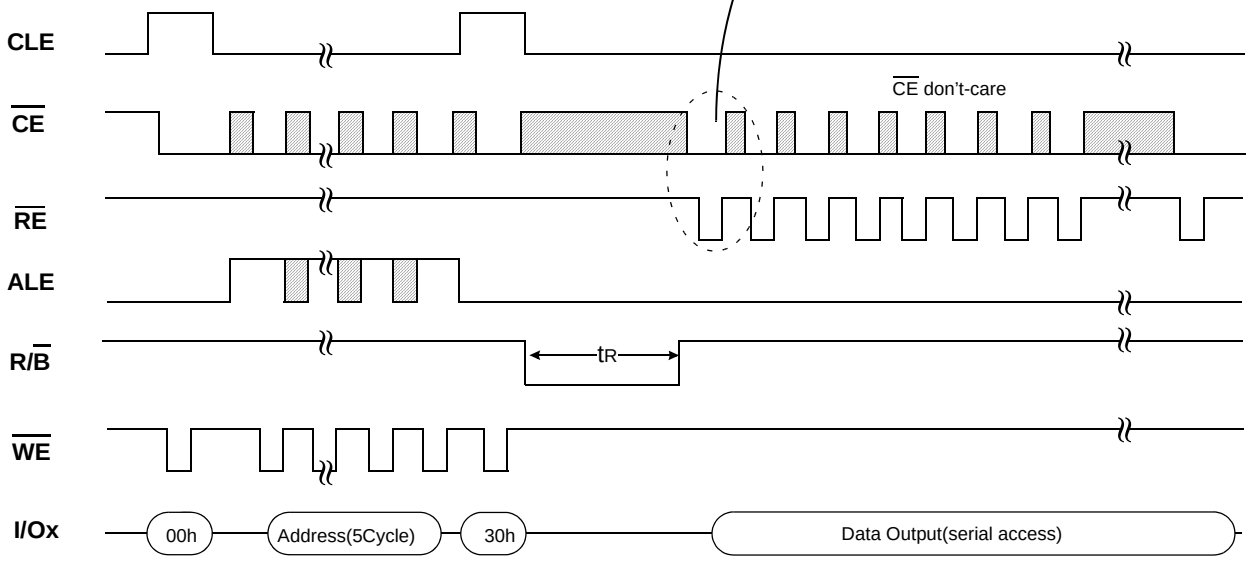
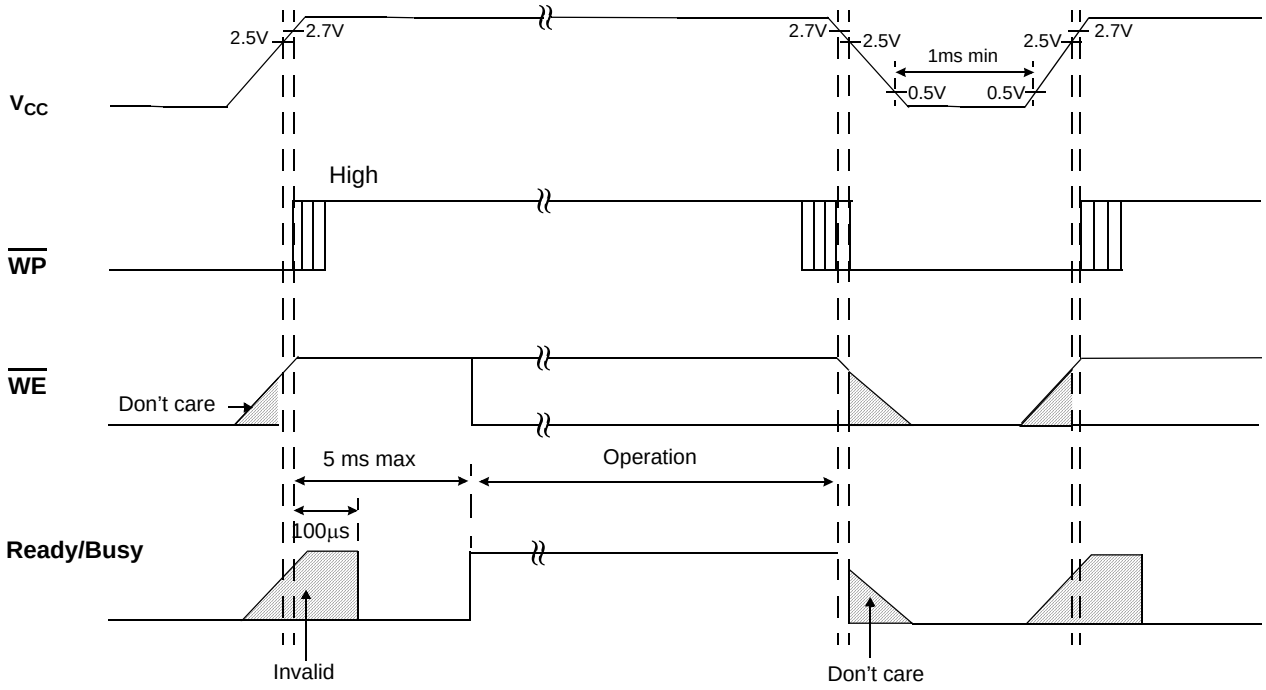


Figure 6. Read Operation with $\overline{CE}$ don't-care

4.0 FUNCTION DESCRIPTION

4.1 Data Protection & Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 2V(3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 100μs is required before internal circuit gets ready for any command sequences as shown in Figure 7. The two step command sequence for program/erase provides additional software protection.



NOTE :
1) During the initialization, the device consumes a maximum current of 30mA (ICC1).
2) Once Vcc drops under 2.5V, Vcc is recommended that it should be driven down to 0.5V and stay low under 0.5V for at least 1ms before Vcc power up.

Figure 7. AC Waveforms for Power Transition

4.2 Mode Selection

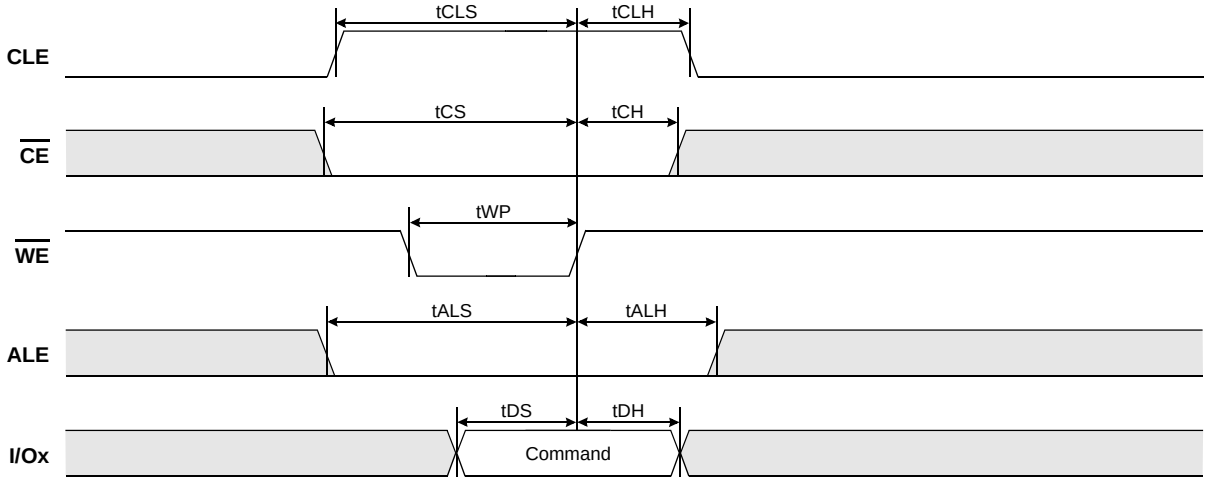
[Table 13] Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⌐↑	H	X	Read Mode	Command Input
L	H	L	⌐↑	H	X		Address Input(5cycles)
H	L	L	⌐↑	H	H	Write Mode	Command Input
L	H	L	⌐↑	H	H		Address Input(5cycles)
L	L	L	⌐↑	H	H	Data Input	
L	L	L	H	↓⌐	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X[1)]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}[2)]	Stand-by	

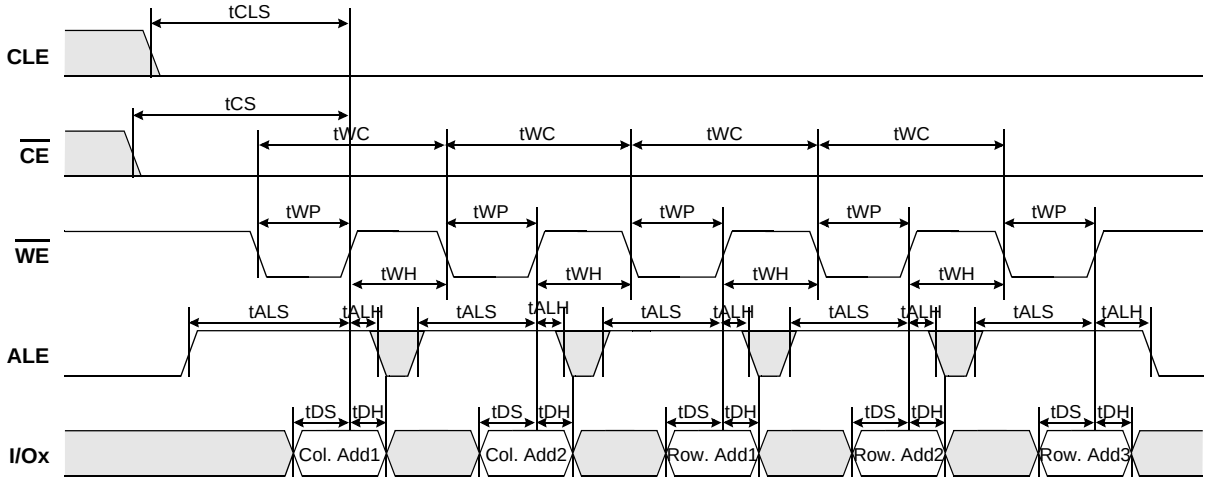
NOTE :
1) X can be V_{IL} or V_{IH}.
2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

4.3 General Timing

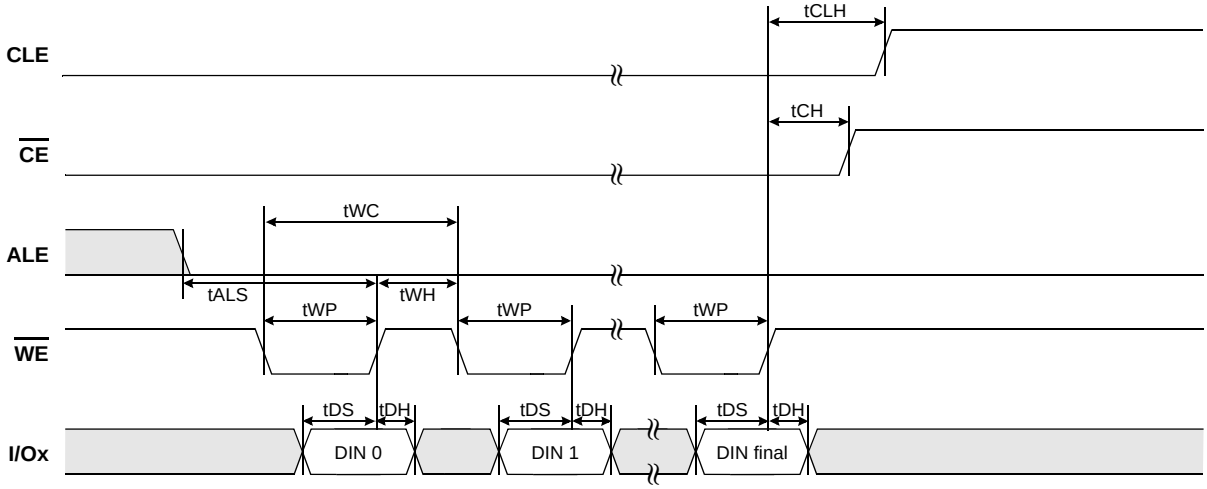
4.3.1 Command Latch Cycle



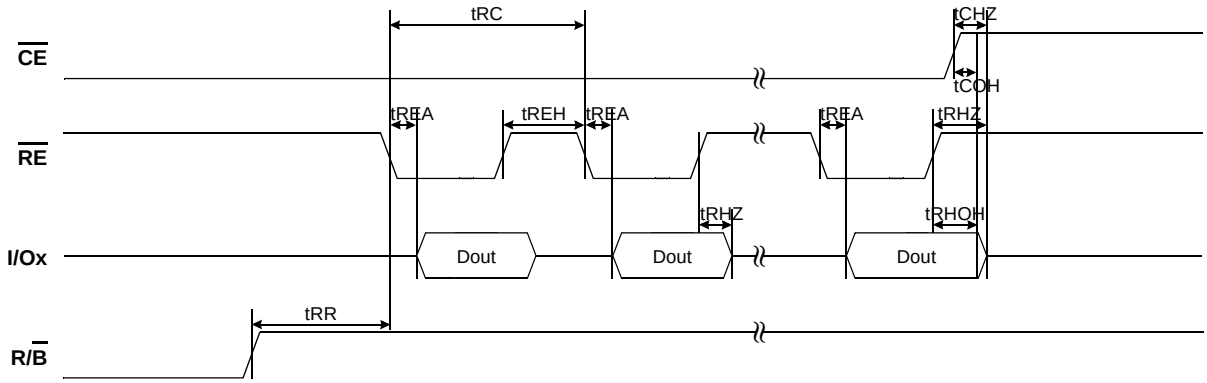
4.3.2 Address Latch Cycle



4.3.3 Input Data Latch Cycle



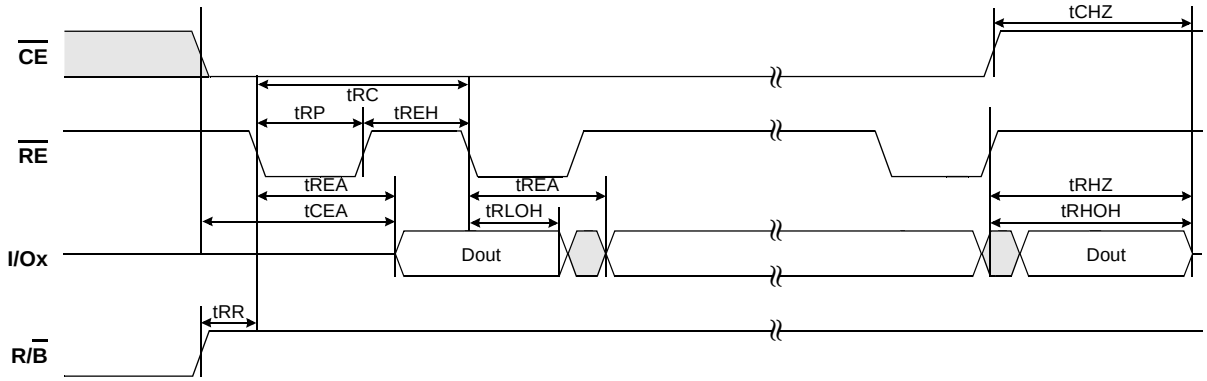
4.3.4 Serial Access Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



NOTE :

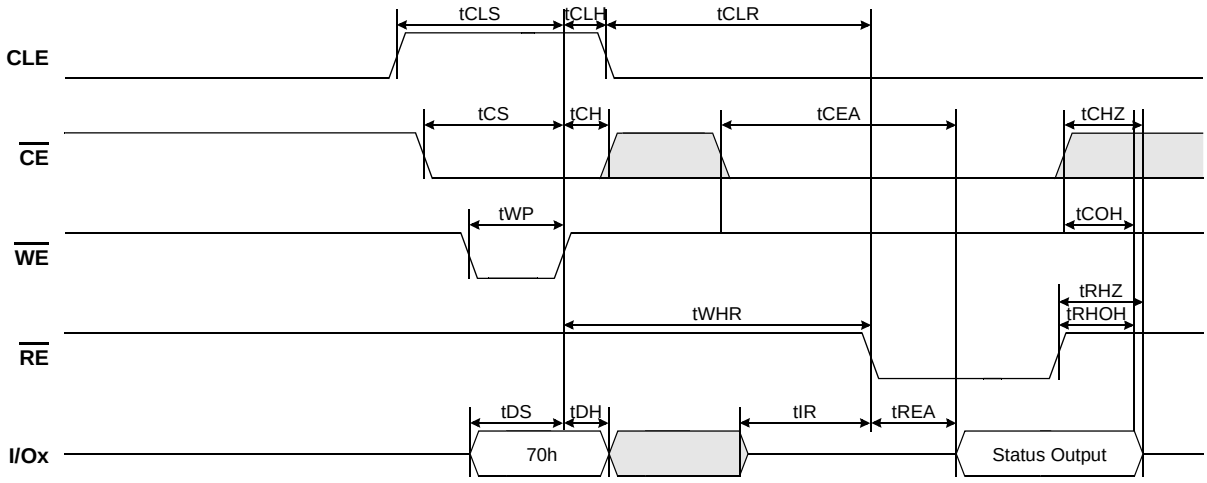
1) Transition is measured at ±200mV from steady state voltage with load.
   This parameter is sampled and not 100% tested.
2) tRHOH starts to be valid when frequency is lower than 20Mhz.

4.3.5 Serial Access Cycle after Read (EDO Type, CLE=L, $\overline{WE}$=H, ALE=L)

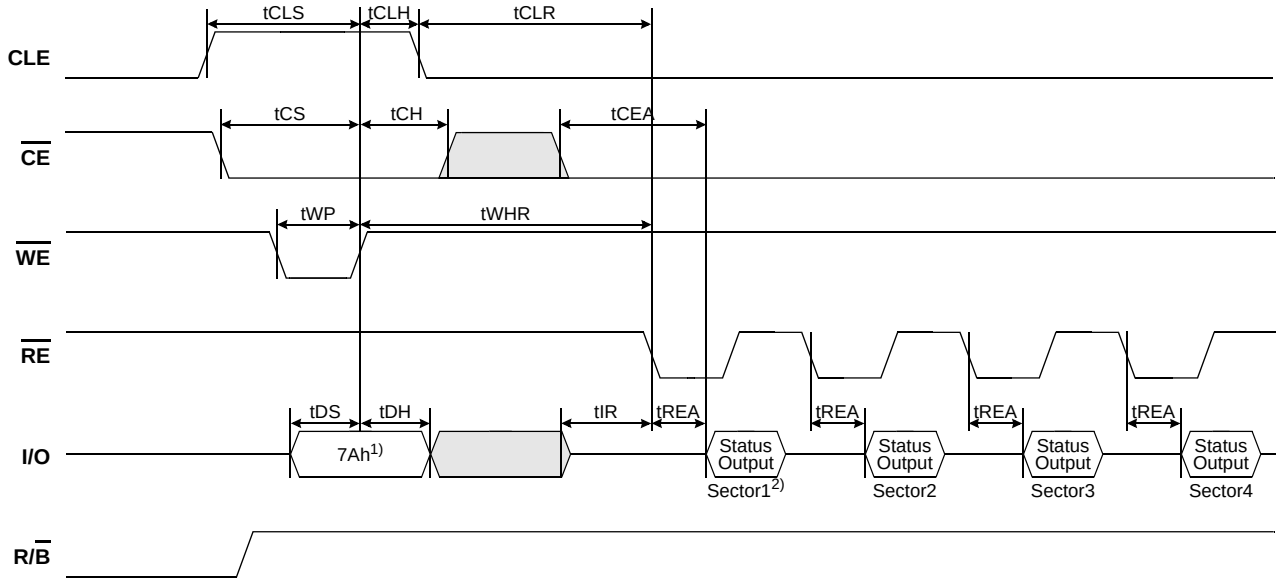


NOTE :
1) Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
2) tRLOH is valid when frequency is higher than 20Mhz.
tRHOH starts to be valid when frequency is lower than 20Mhz.

4.4 Read Status Cycle

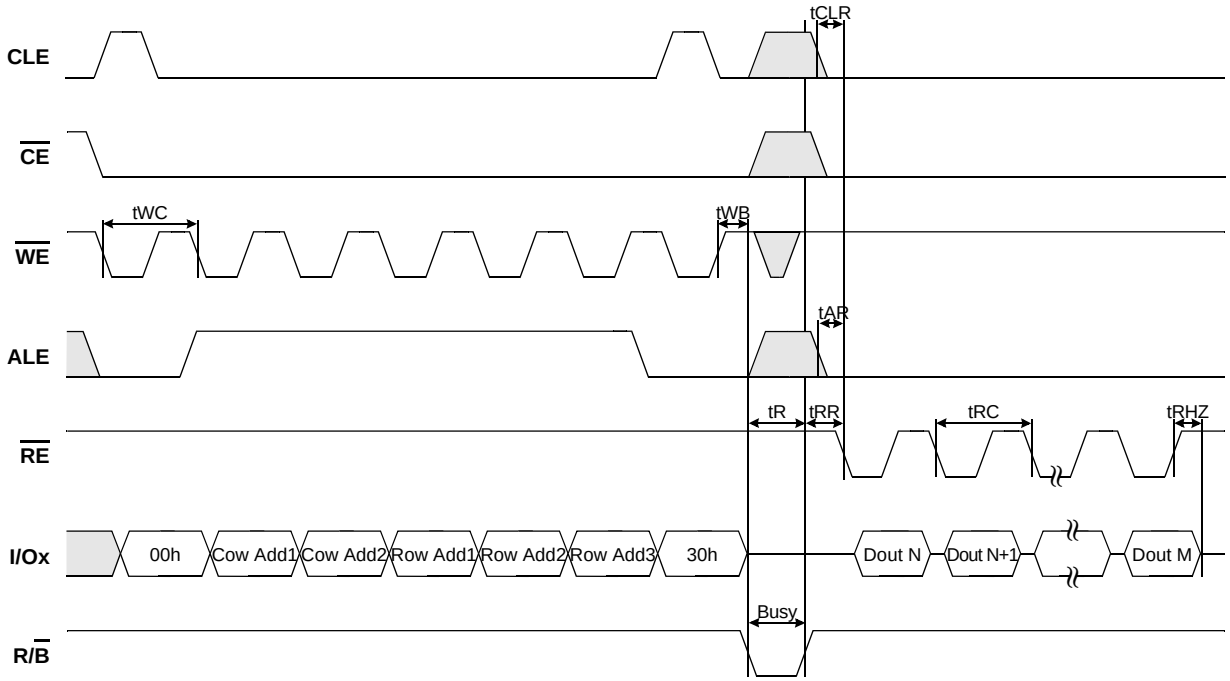


4.5 ECC Read Status Cycle

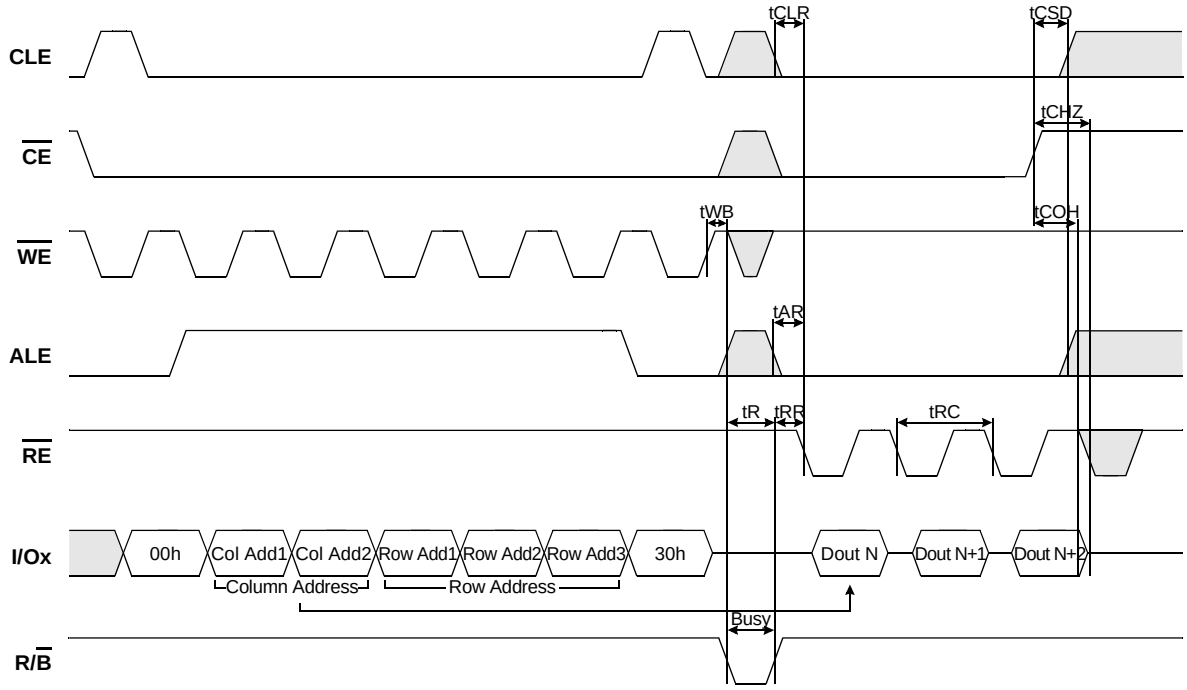


NOTE :
1) ECC Read Status output should include all 4 sector information.

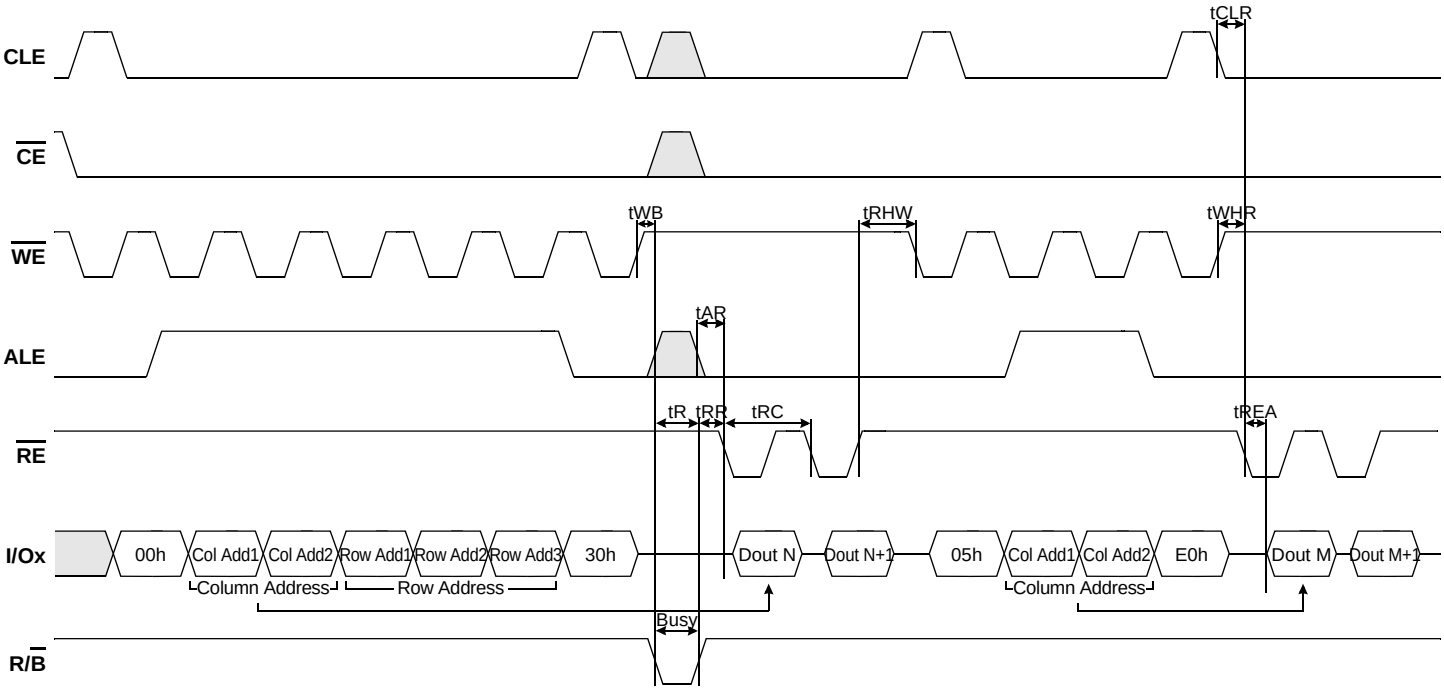
4.6 Read Operation



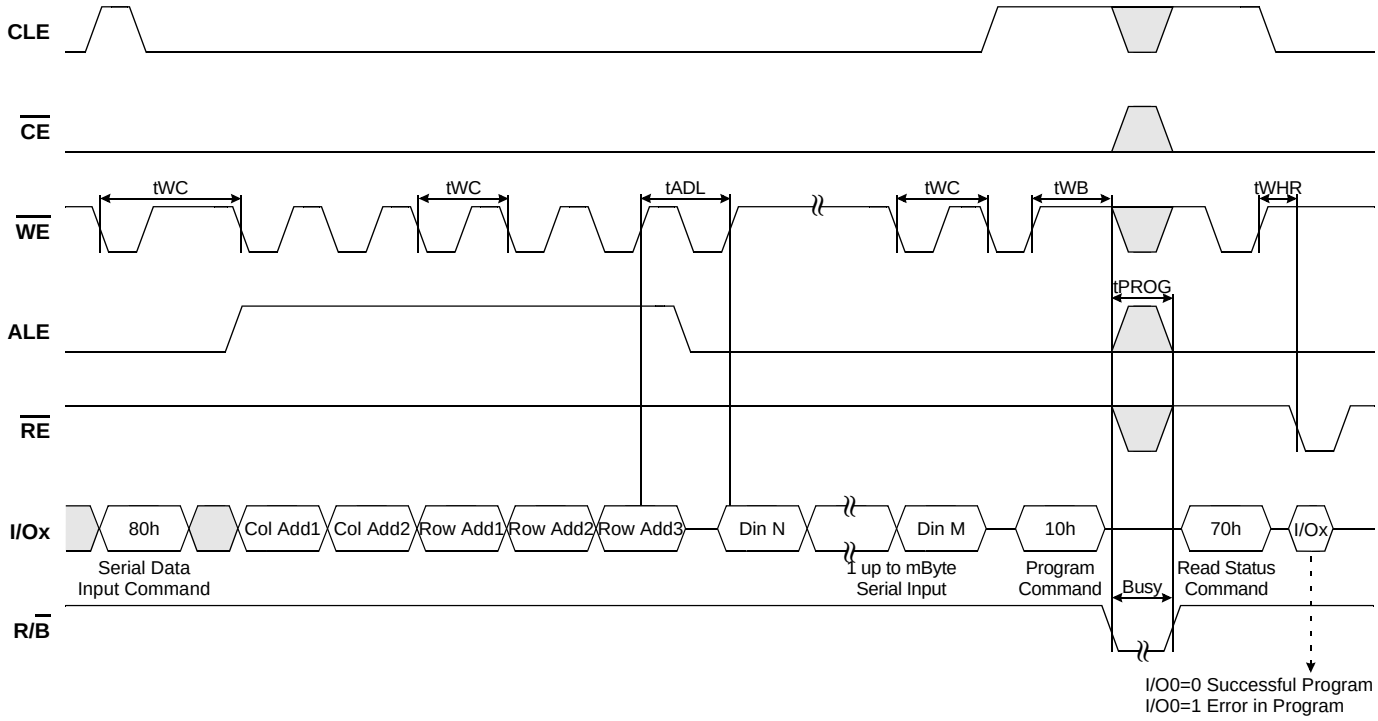
4.7 Read Operation (Intercepted by $\overline{CE}$)



4.8 Random Data Output In a Page Operation

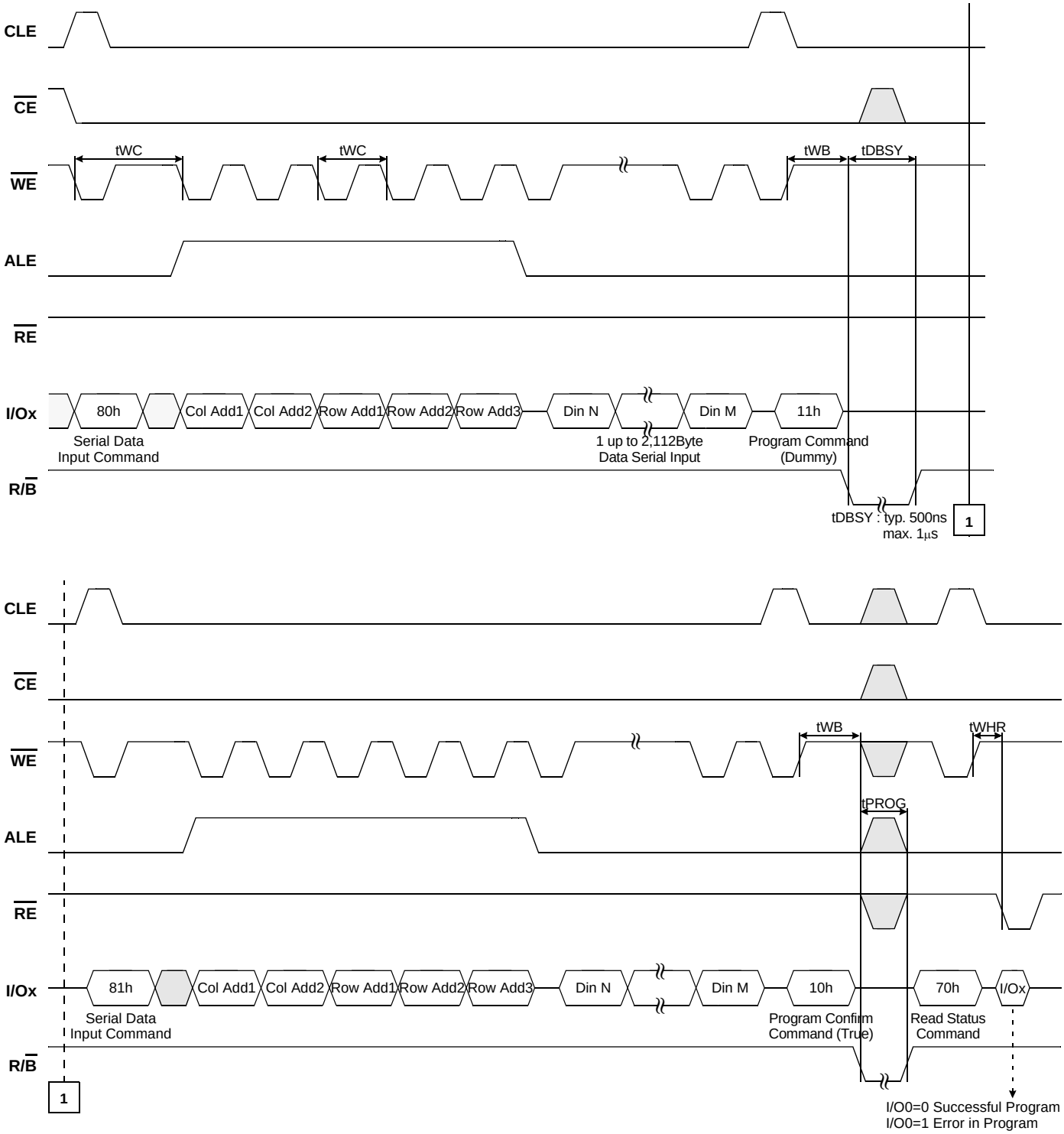


4.9 Page Program Operation

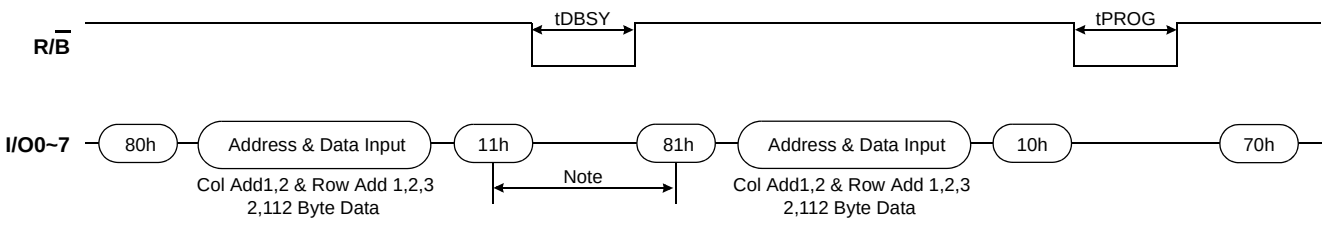


NOTE :
tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

4.10 Two-Plane Page Program Operation

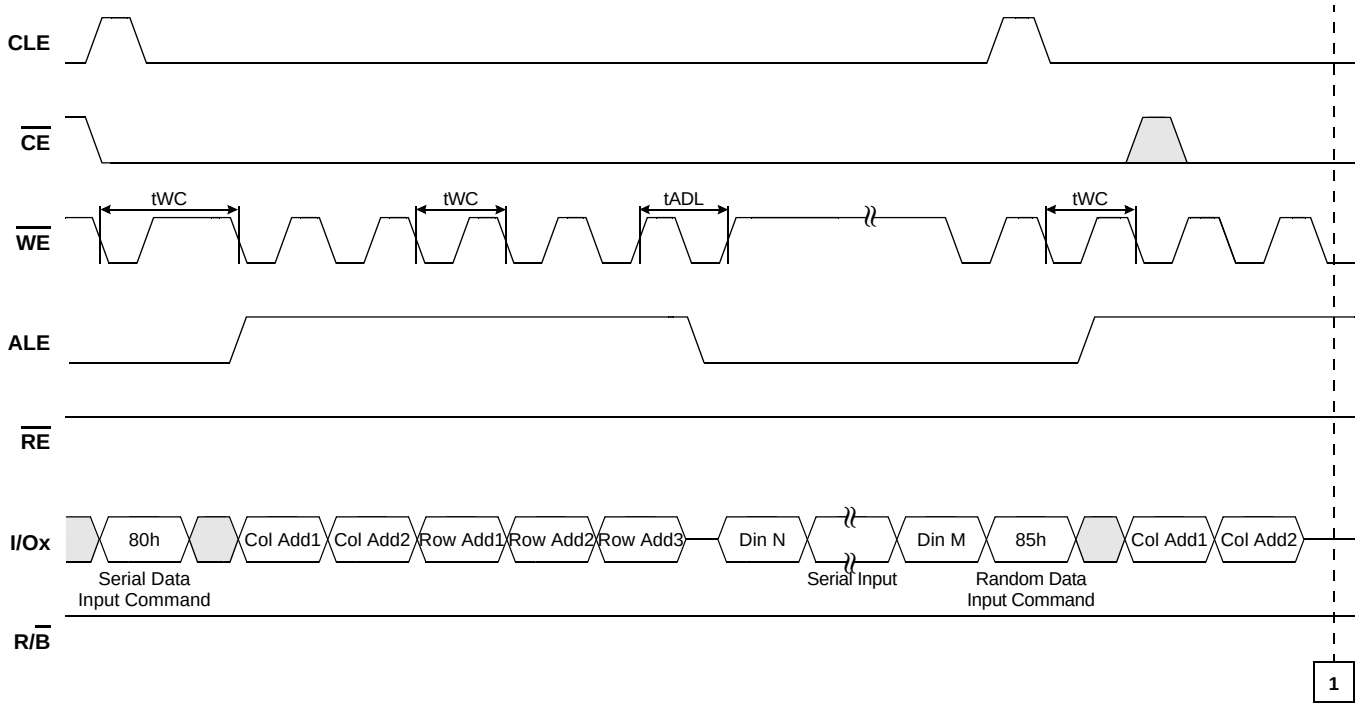


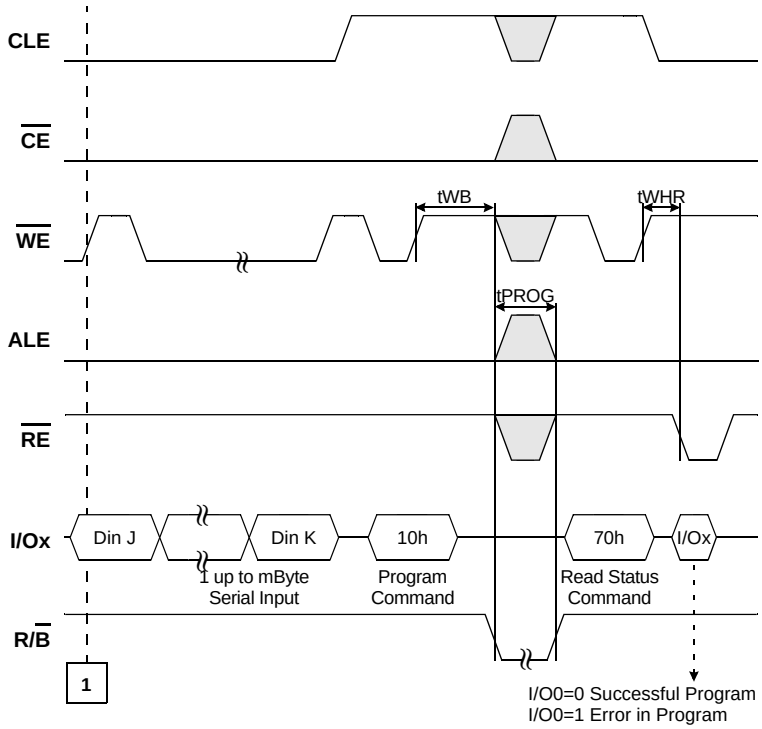
Ex.) Two-Plane Page Program



NOTE :
Any command between 11h and 81h is prohibited except 70h and FFh.

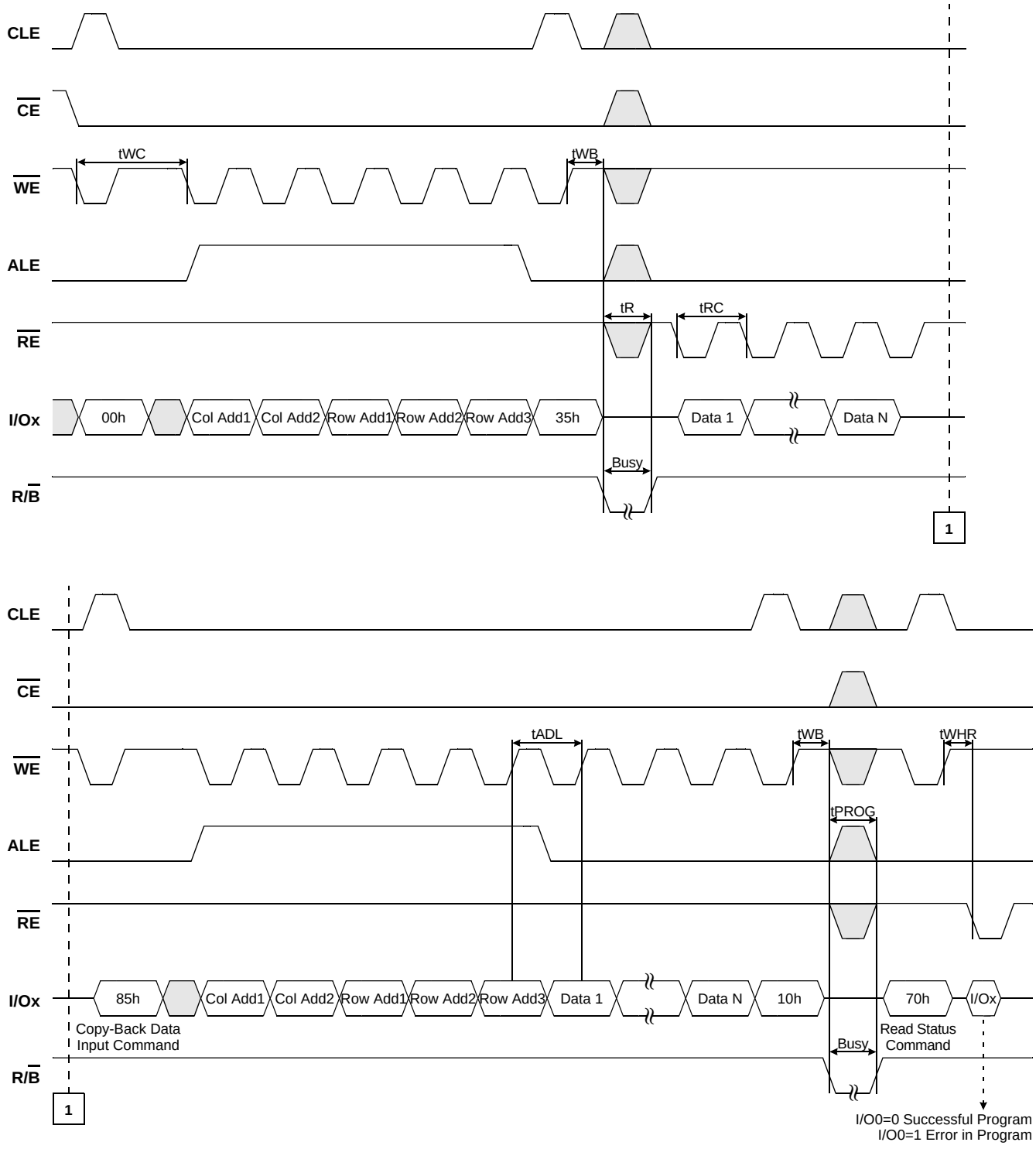
4.11 Program Operation with Random Data Input Operation



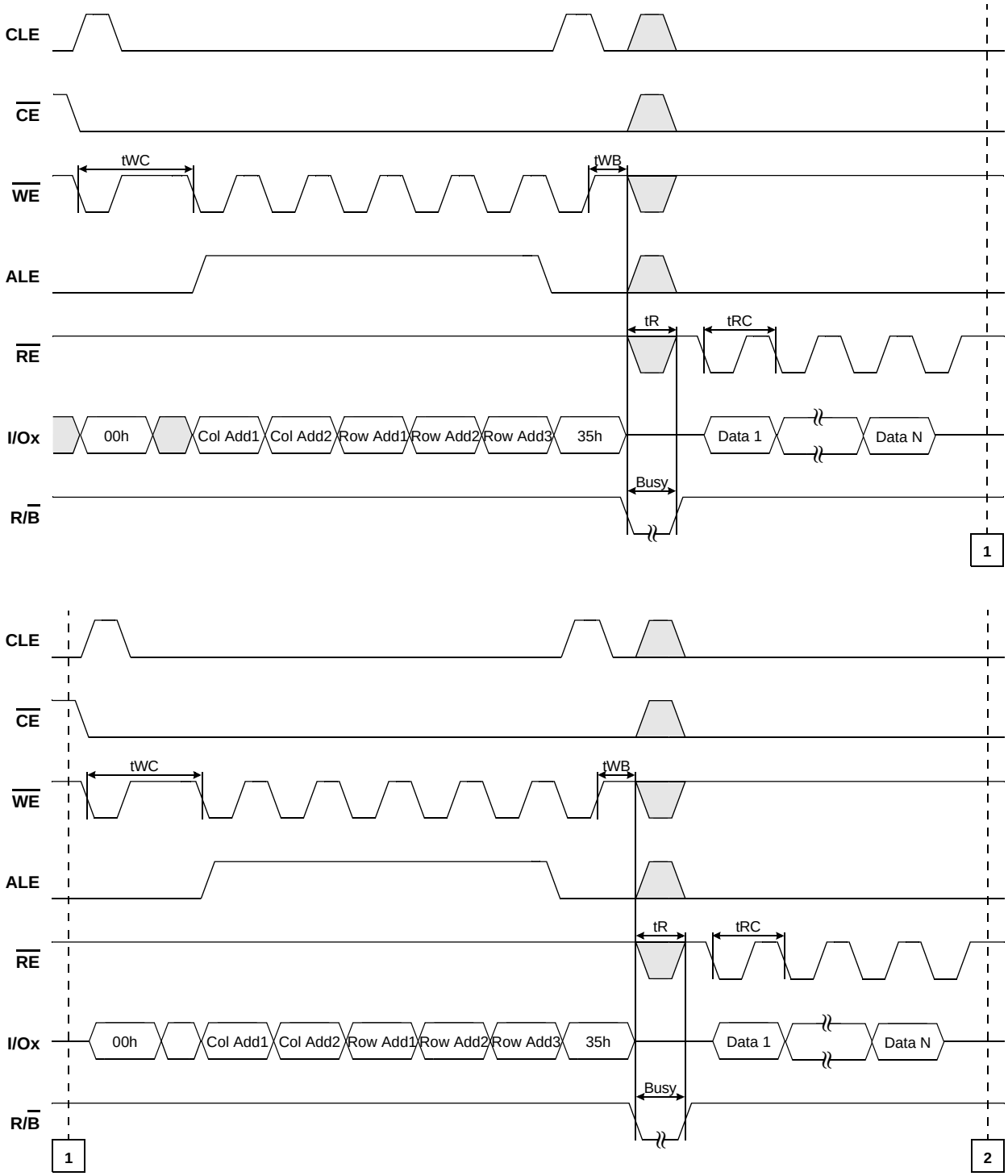


NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

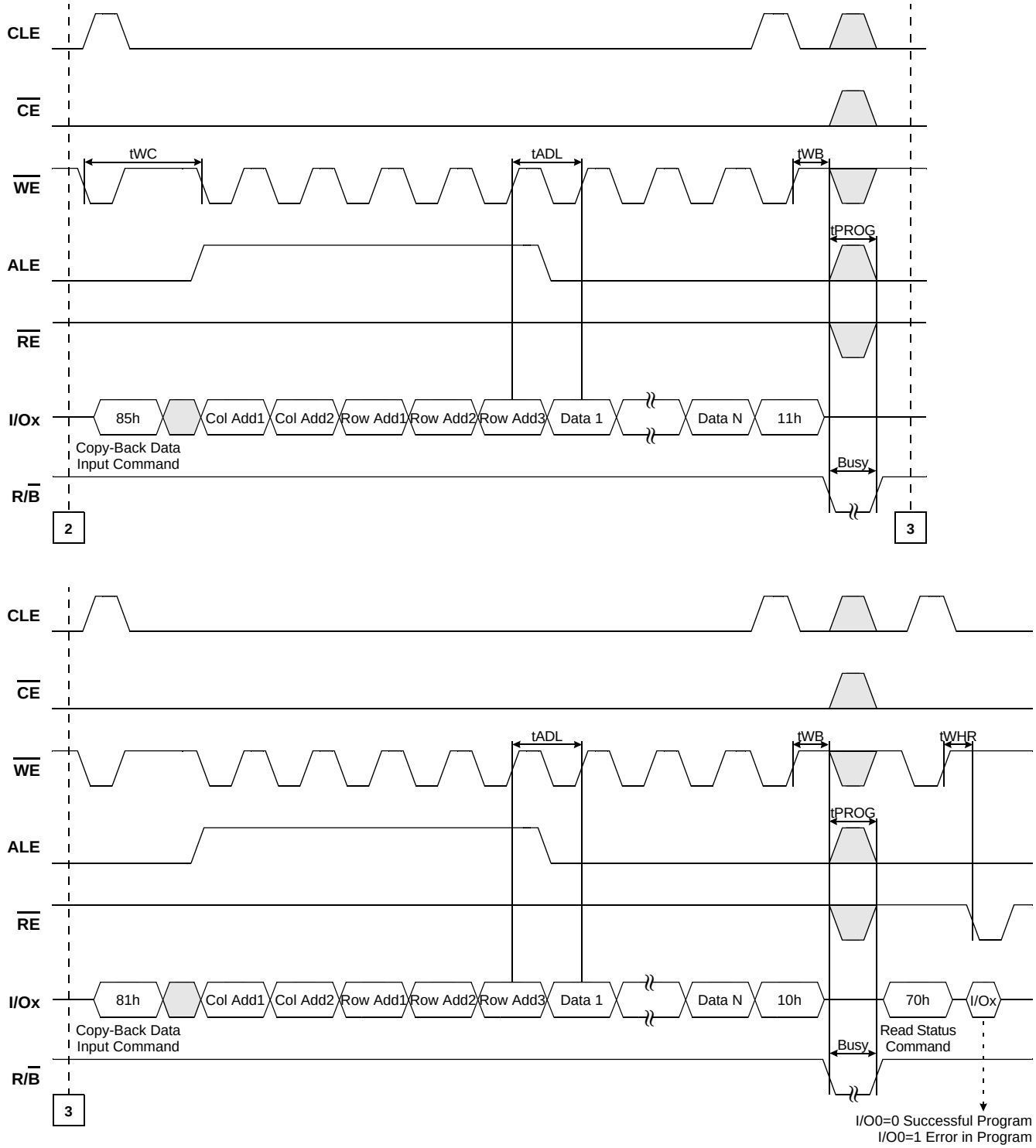
4.12 Copy-Back Program Operation



4.13 Two-Plane Copy-Back Program Operation(1/2)

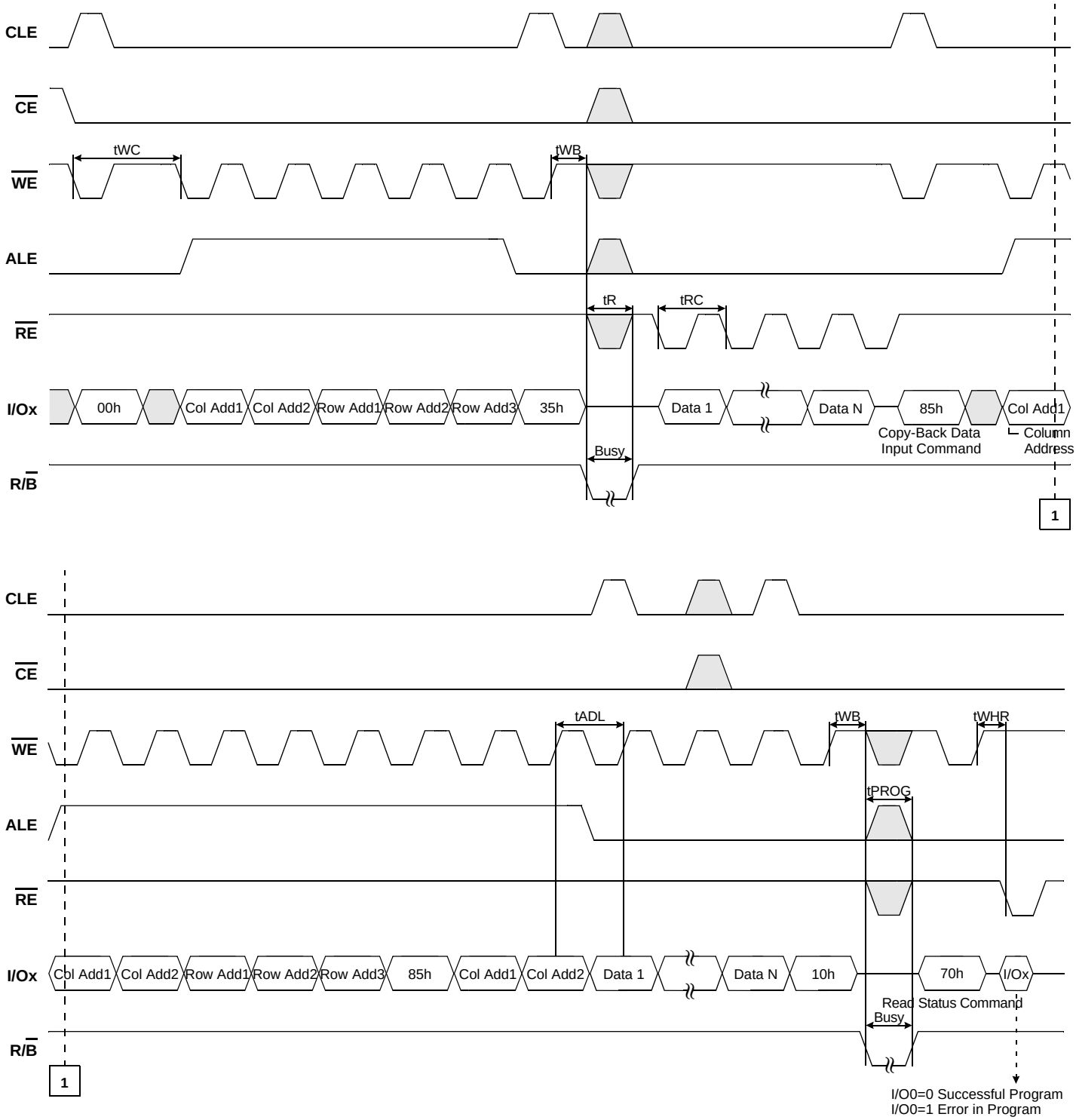


4.14 Two-Plane Copy-Back Program Operation(2/2)



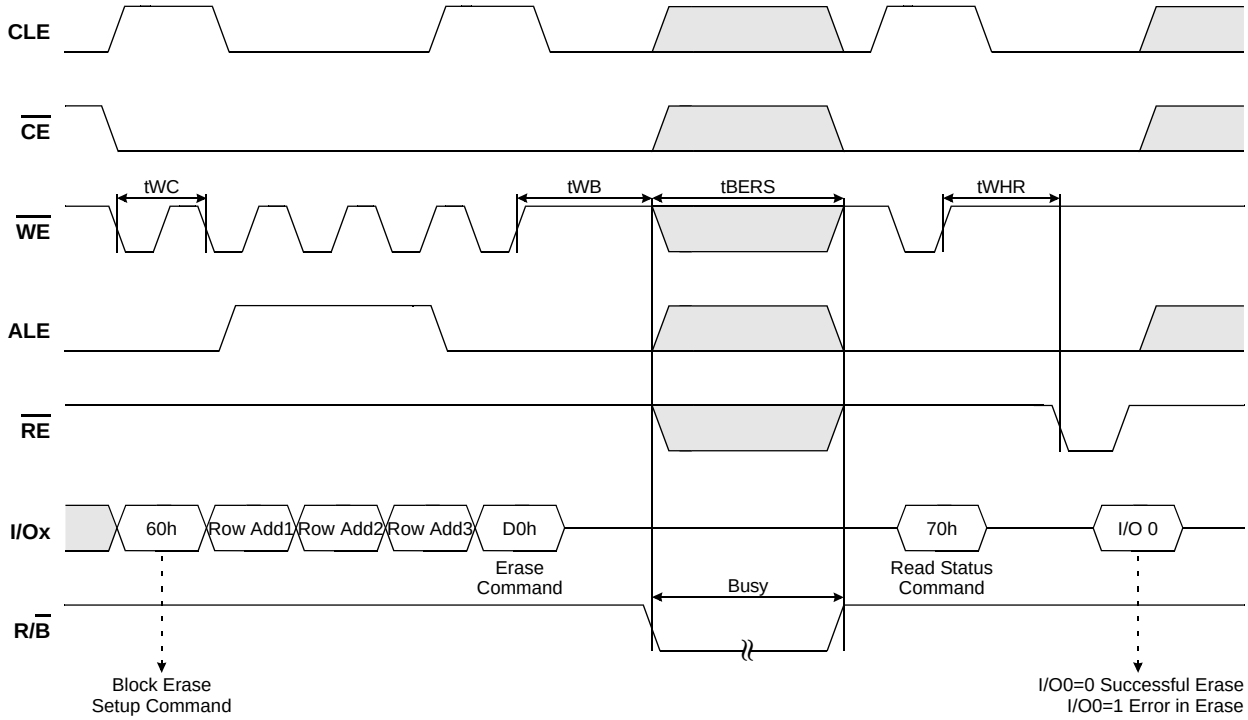
NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

4.15 Copy-Back Program Operation with Random Data Input Operation

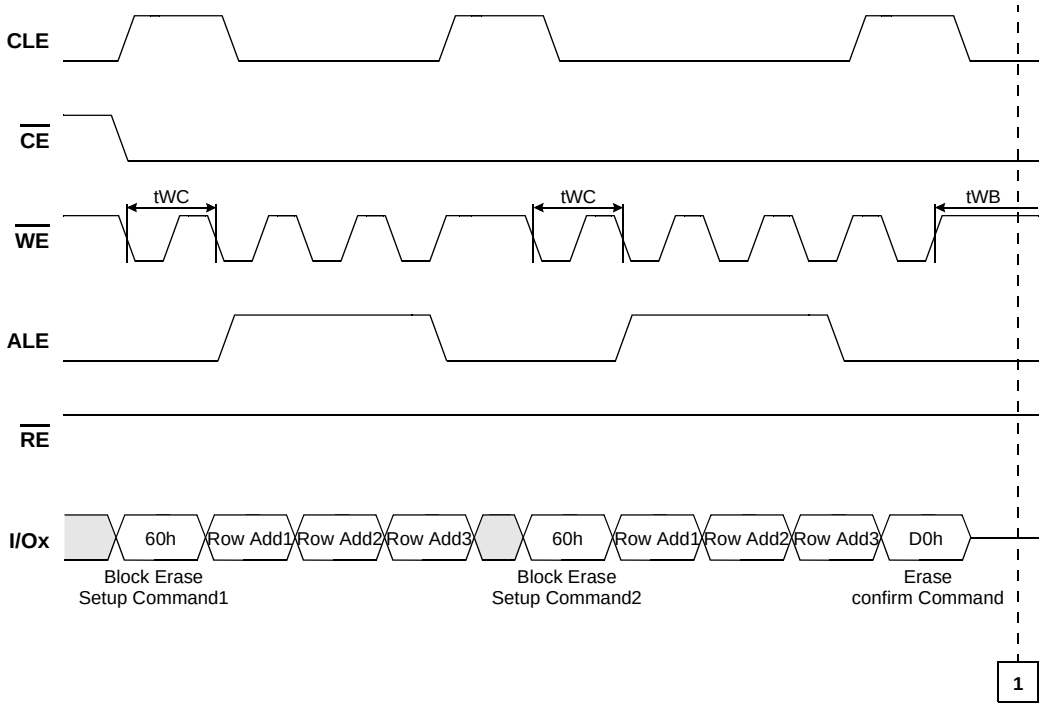


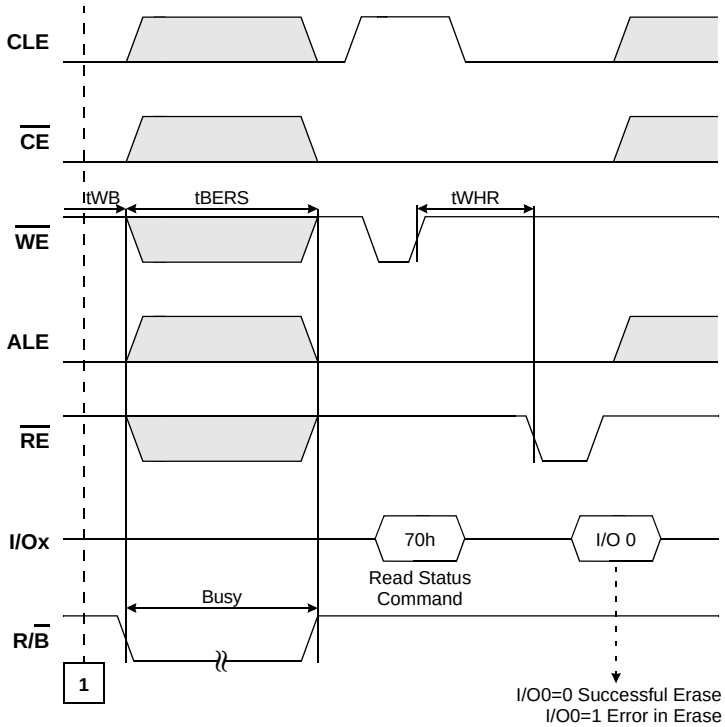
NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
2) Copy-Back Program operation is allowed only within the same memory plane.

4.16 Block Erase Operation

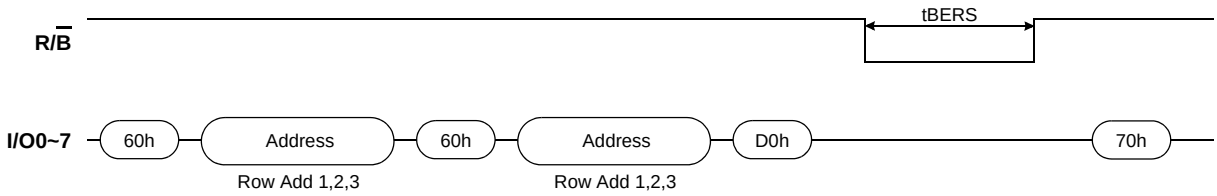


4.17 Two-Plane Block Erase Operation

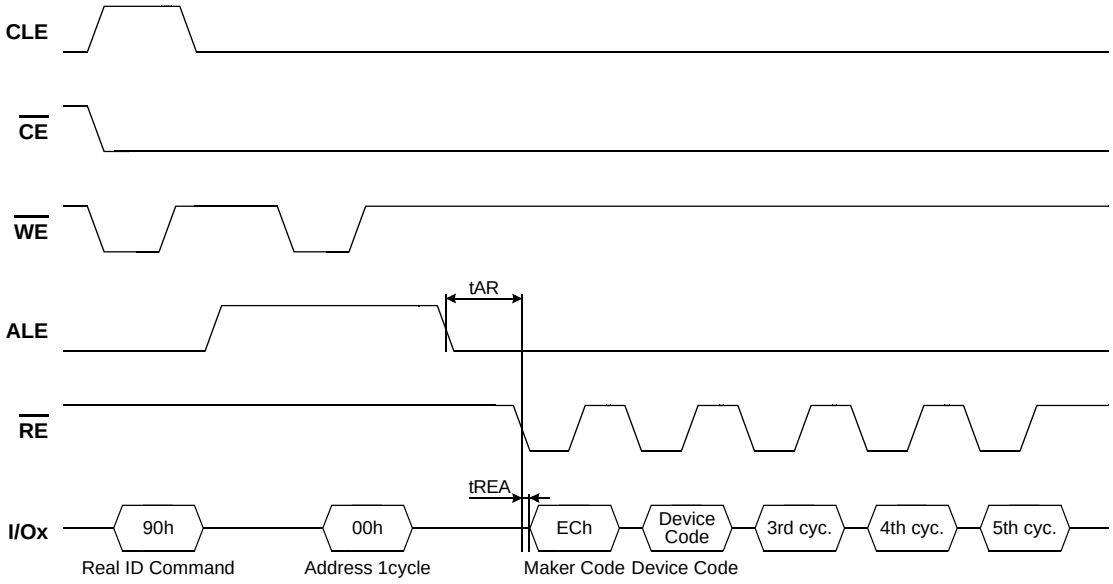




Ex.) Address Restriction for Two-Plane Block Erase Operation



4.18 Read ID Operation



5.0 DEVICE OPERATION

5.1 Page Read Operation

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 25μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

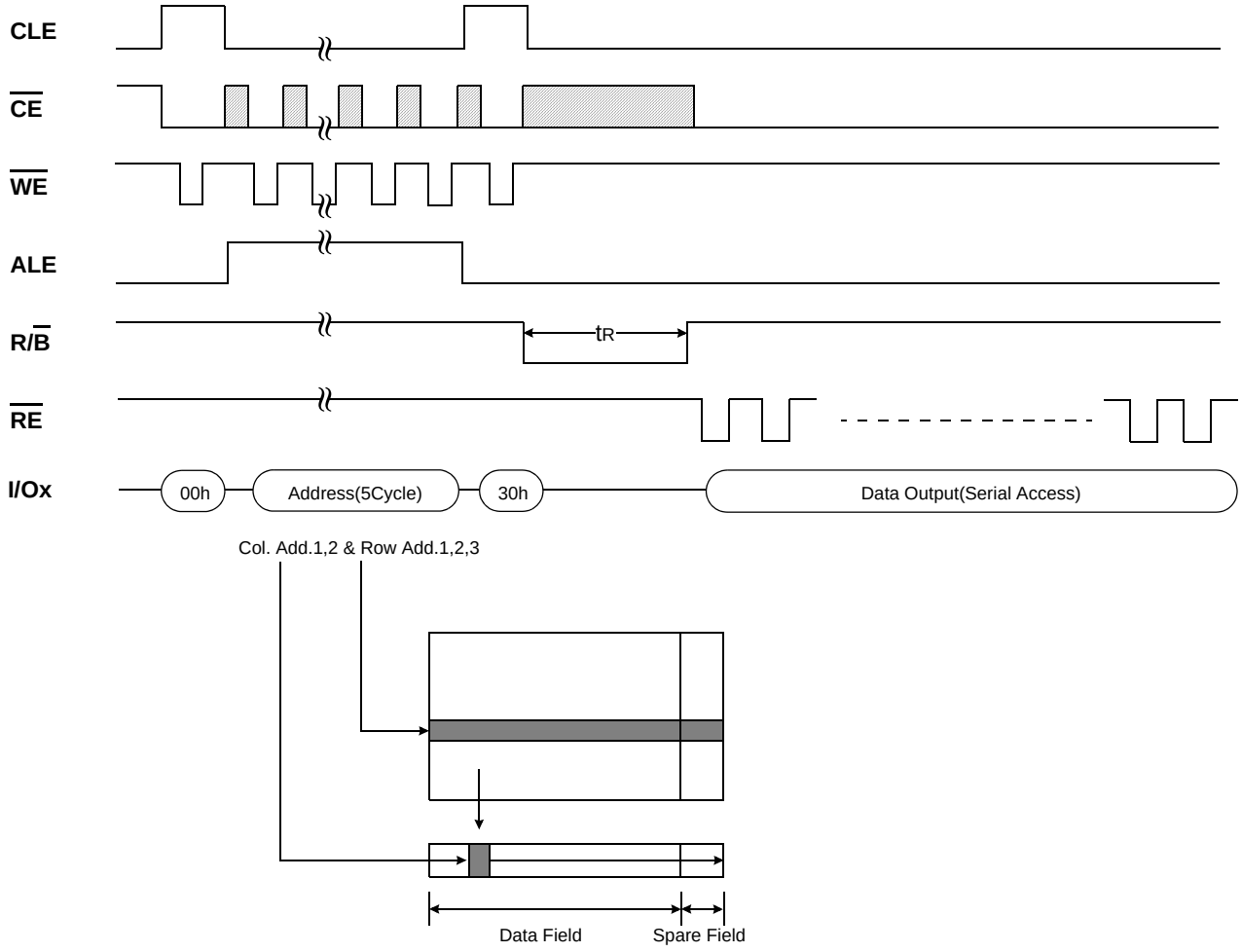


Figure 8. Page Read Sequence

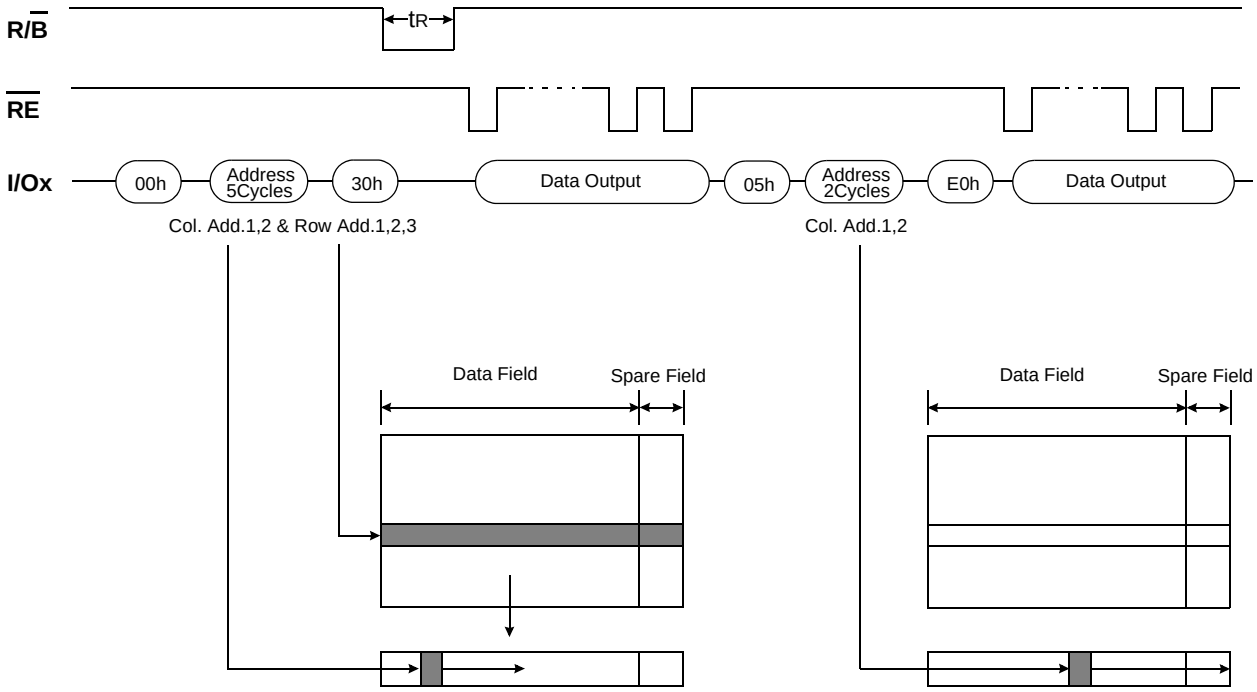


Figure 9. Page Read with Random Data Output Sequence

5.2 Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased.
The addressing should be done in sequential order in a block. A page program cycle consist of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status bit(I/O 0) may be checked(Figure 10). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

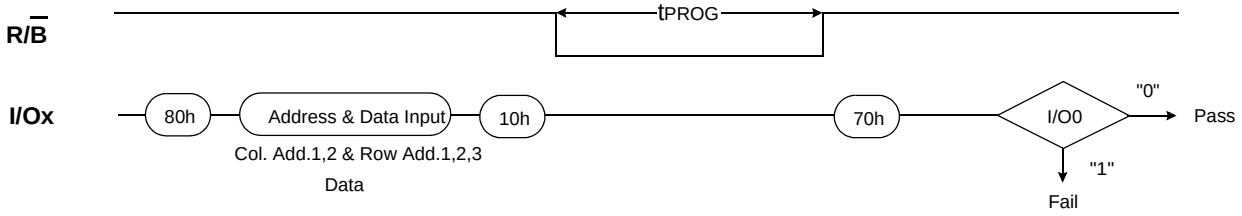


Figure 10. Page Program Sequence

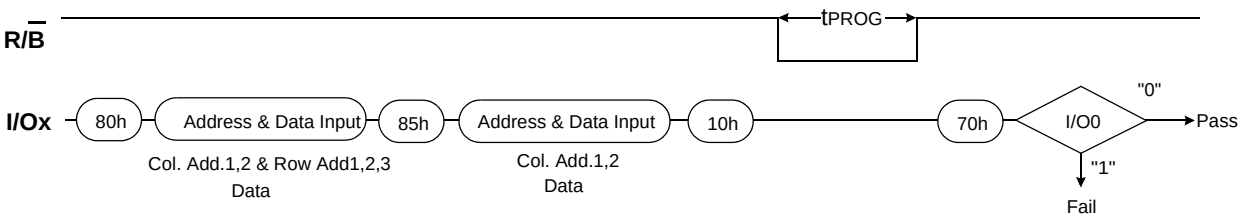


Figure 11. Program Operation with Random Data Input Sequence

5.3 Copy-Back Program Operation

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data re-loading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status bit(I/O 0) may be checked(Figure 12 & Figure 10). The command register remains in Read Status command mode until another valid command is written to the command register.
During copy-back program, data modification is possible using random data input command (85h) as shown in Figure 10.

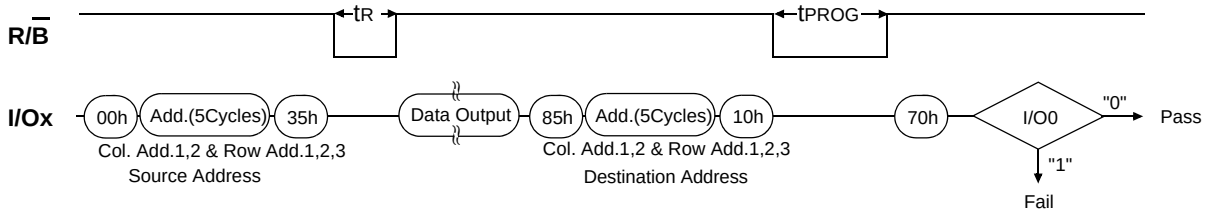


Figure 12. Copy-Back Program Sequence

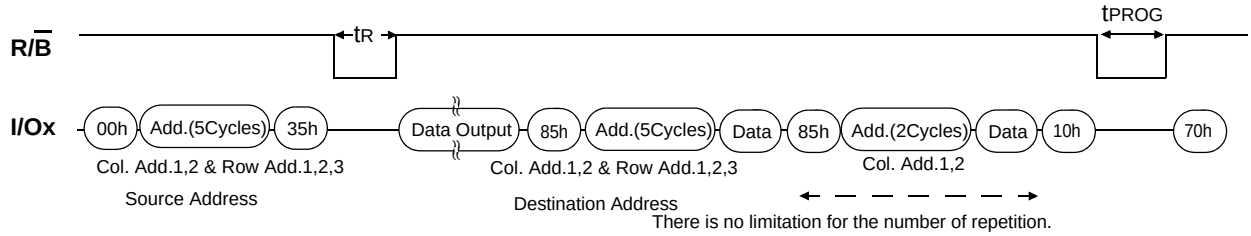


Figure 13. Copy-Back Program with Random Data Input Sequence

NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.

5.4 Block Erase Operation

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{18} to A_{29} is valid while A_{12} to A_{17} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status bit(I/O 0) may be checked. Figure 14 details the sequence.

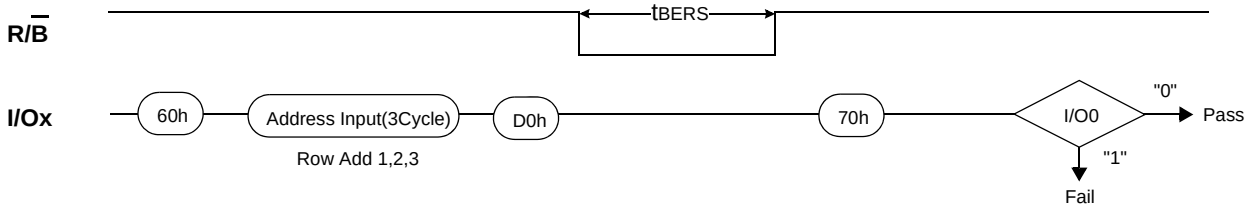


Figure 14. Block Erase Sequence

5.5 Unaligned Two-Plane Operation

Two-Plane Read/Program operation is supported in unaligned block addresses, as long as page addresses are same in all planes.

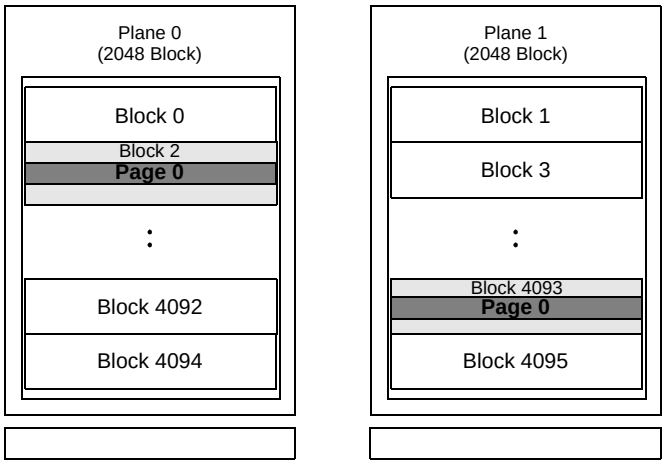
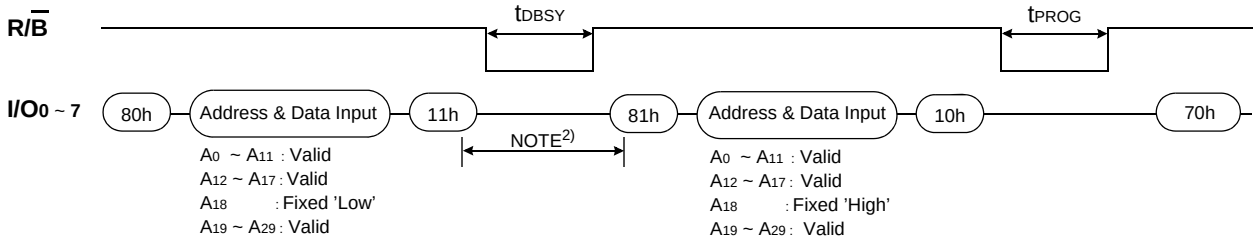


Figure 15. Example of Unaligned Two-Plane Operation

5.6 Two-Plane Page Program Operation

Two-Plane Page Program is an extension of Page Program, for a single plane with 2112 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages.
After writing the first set of data up to 2112 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program command (10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, R/$\overline{B}$ remains in Busy state for a short period of time(tDBSY). Read Status command (70h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for the other plane is inputted after the 81h command and address sequences. After inputting data for the last plane, actual True Page Program(10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/$\overline{B}$ and Read Status is the same as that of Page Program. Althougth two planes are programmed simultaneously, pass/fail is not available for each page when the program operation completes. Status bit of I/O 0 is set to "1" when any of the pages fails.
Restriction in addressing with Two-Plane Page Program is shown is Figure 13.



NOTE :
1) It is noticeable that same row address except for A18 is applied to the two blocks.
2) Any command between 11h and 81h is prohibited except 70h and FFh.

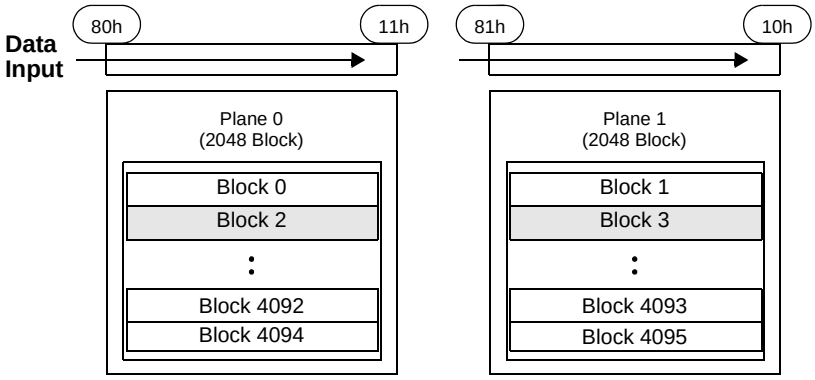


Figure 16. Two-Plane Page Program Sequence

5.7 Two-Plane Copy-Back Program Operation

Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 2112 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages.

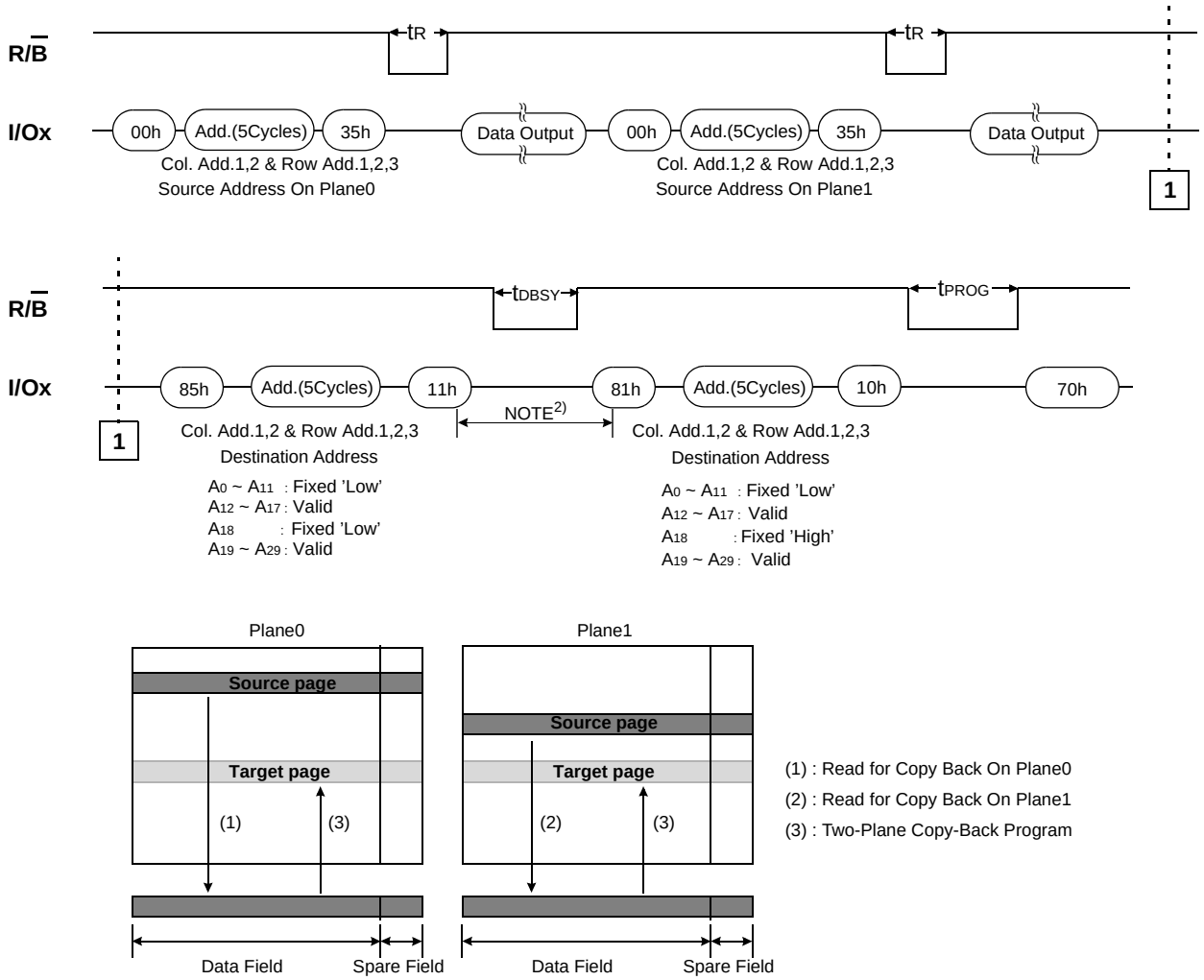


Figure 17. Two-Plane Copy-Back Program Sequence

NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
2) Any command between 11h and 81h is prohibited except 70h and FFh.

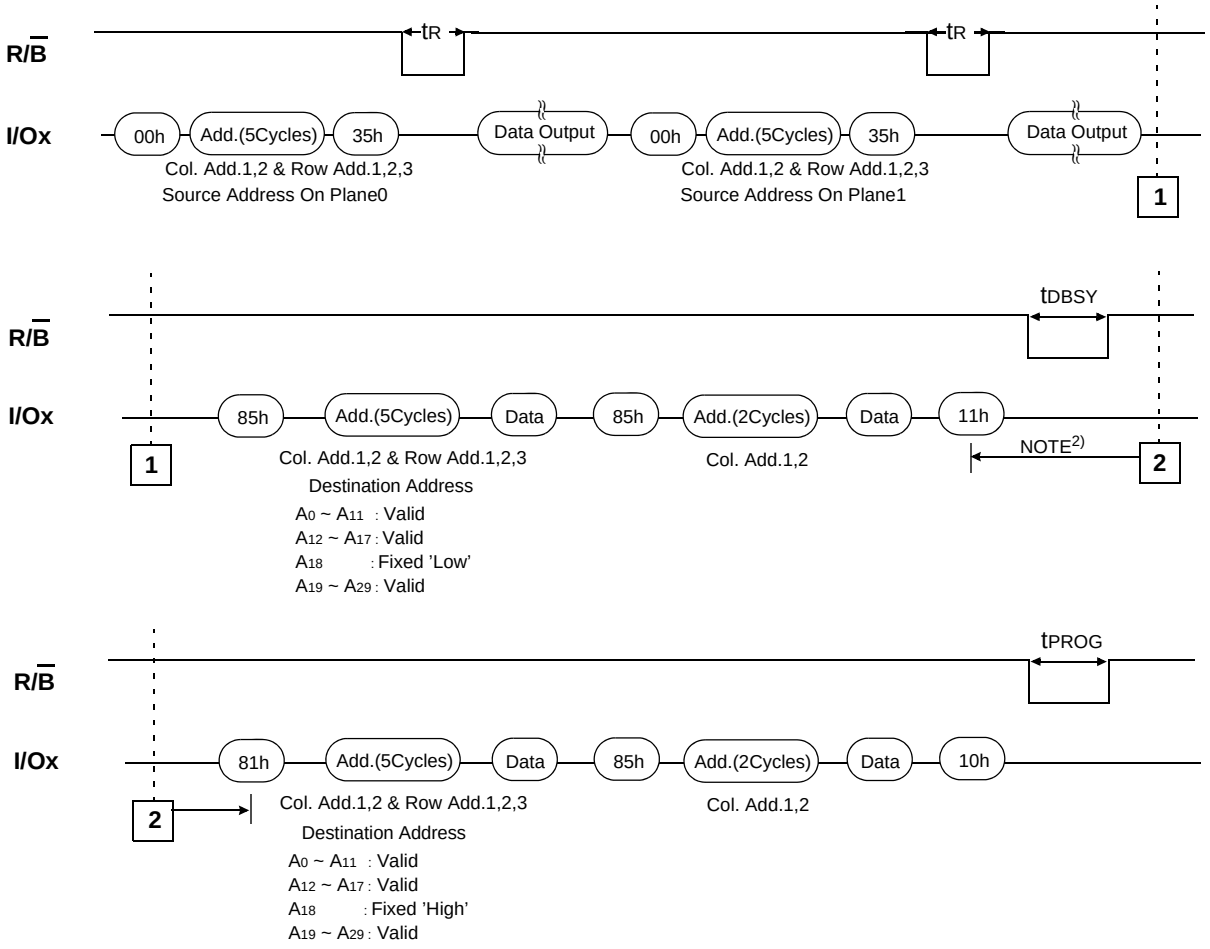


Figure 18. Two-Plane Copy-Back Program Operation with Random Data Input Sequence

NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
2) Any command between 11h and 81h is prohibited except 70h and FFh.

5.8 Two-Plane Block Erase Operation

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command(60h) followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command(D0h) initiates the actual erasing process. The completion is detected by monitoring R/$\overline{B}$ pin or Ready/Busy status bit (I/O 6).

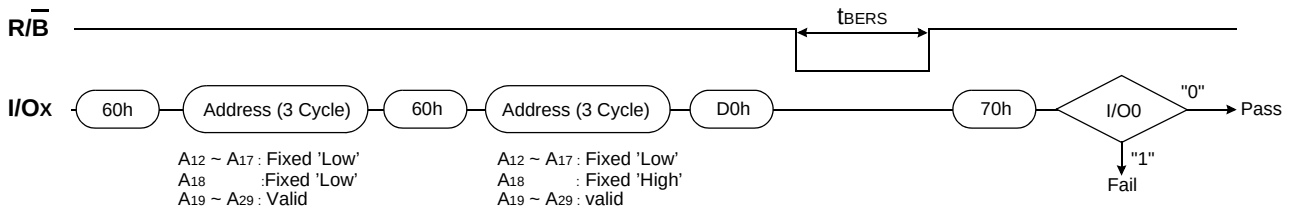


Figure 19. Two-Plane Block Erase Sequence

5.9 Read Status

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 14 for specific Status Register definitions and Table 15 for specific F1h/F2h Status Register definitions. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

[Table 14] Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Not use	Don't -cared
I/O 2	Not use	Not use	Not use	Don't -cared
I/O 3	Not use	Not use	Normal or uncorrectable / Recommended to rewrite	Chip Read Status Normal or uncorrectable : 0 Recommended to rewrite : 1
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :
1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

[Table 15] Status Register Definition for F1h and F2h Command

I/O No.	Page Program	Block Erase	Read	Definition
I/O 0	Chip Pass/Fail	Chip Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Plane0 Pass/Fail	Plane0 Pass/Fail	Not Use	Pass : "0" Fail : "1"
I/O 2	Plane1 Pass/Fail	Plane1 Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 3	Not use	Not use	Normal or uncorrectable / Recommended to rewrite	Chip Read Status Normal or uncorrectable : 0 Recommended to rewrite : 1
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :
1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

5.10 ECC Read Status

Using the ECC Read Status function, the Error Correction Status can be identified.
ECC is performed on the NAND Flash main and spare areas.
The ECC Read Status function also shows the number of errors in a sector as identified from a ECC check in during a read operation.

7	6	5	4	3	2	1	I/O0
Sector Information				ECC Status			

[Table 16] ECC Status

I/O3 to I/O0	ECC Status
0000	No Error
0001	1bit error (Correctable)
0010	2bit error (Correctable)
0011	3bit error (Correctable)
0100	4bit error (Correctable)
Others	Reserved

[Table 17] Sector Information

I/O7 to I/O4	Sector Information
0000	1st Sector (Main and Spare area)
0001	2nd Sector (Main and Spare area)
0010	3rd Sector (Main and Spare area)
0011	4th Sector (Main and Spare area)
Others	Reserved

5.11 ECC Sector Information

ECC is generated by internal ECC.
During Read operation, the device automatically executes ECC. After read operation is executed, read status command can be issued to identify the read status the read status remains unmodified until other valid commands are executed.

[Table 18] 2KByte Page Assignment

1'st Main	2'nd Main	3'rd Main	4'th Main	1'st Spare	2'nd Spare	3'rd Spare	4'th Spare
512B	512B	512B	512B	16B	16B	16B	16B

[Table 19] Definition of 528Byte Sector

Sector	Column Address (Byte)	
	Main Field	Spare Field
1'st Sector	0 ~ 511	2,048 ~ 2,063
2'nd Sector	512 ~ 1,023	2,064 ~ 2,079
3'rd Sector	1,024 ~ 1,535	2,080 ~ 2,095
4'th Sector	1,536 ~ 2,047	2,096 ~ 2,111

NOTE :
1) The internal ECC manages all data of Main area and Spare area.
2) A sector is the minimum unit for program operation and the number of program per page must not exceed 4.

5.12 Partial Page Program Information

Each Sector can be programmed individually as defined Figure 17.

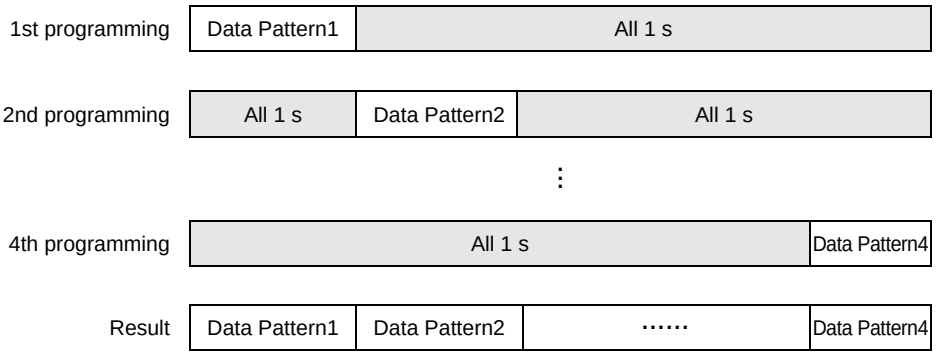


Figure 20. Partial Page Program Guide

NOTE :
1) A sector in the minimum unit for program operation and the number of program per page must not exceed 4.

5.13 Read ID

5.13.1 00h Address ID Definition

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 21 shows the operation sequence.

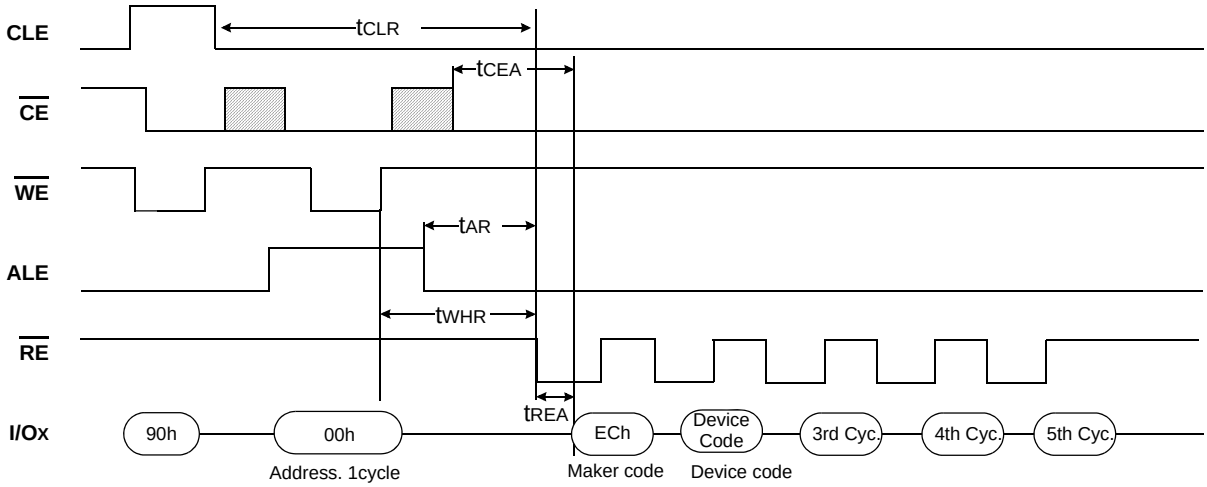


Figure 21. Read ID sequence

5.13.1.1 00h Address ID Cycle

[Table 20] 00h Address ID cycle

Device	Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle
DNS4G08U0F	DCh	10h	95h	56h
DNS8G08U0F	D3h	51h		5Ah

NOTE :
1) When reading the 6th cycle of Read ID, may acquire the "ECh" vlalue.

[Table 21] 00h Address ID Definition Table

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc
4th Byte	Page Size, Block Size, Redundant Area Size, Organization, Serial Access Minimum
5th Byte	Plane Number, Plane Size

[Table 22] 3rd ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

[Table 23] 4th ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 0 1 1 0 1 1			
Redundant Area Size (byte/512byte)	8 16					0 1	
Organization	x8 x16		0 1				
Serial Access Minimum	50ns/30ns 25ns Reserved Reserved	0 1 0 1			0 0 1 1		

[Table 24] 5th ID Data

	Description	I/O7	I/O6 I/O5 I/O4	I/O3 I/O2	I/O1	I/O0
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1		
Plane Size (w/o redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1			
Process	21nm 1ynm Reserved Reserved				0 1 0 1	1 0 0 1
Reserved		0			0	0

5.14 Reset Operation

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin changes to low for tRST after the Reset command is written. Refer to Figure 22 below.

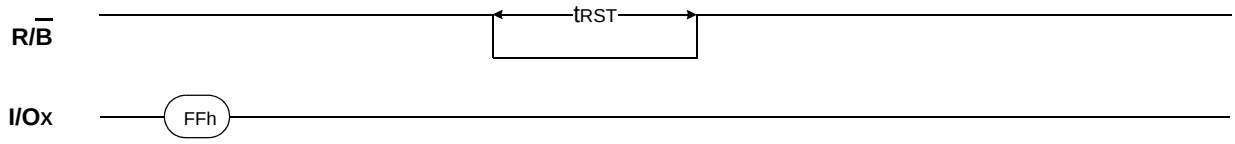


Figure 22. Reset Sequence

[Table 25] Device Status

	After Power-up	After Reset
Operation mode Mode	00h Command is latched	Waiting for next command

5.15 Interleave Operation

DNS8G08U0F is composed of two DNS4G08U0Fs. DNS8G08U0F provides interleaving operation between two DNS4G08U0Fs.

This interleaving page program improves the system throughput almost twice compared to non-interleaving page program.

At first, the host issues page program command to one of the DNS4G08U0F chips, say DNS4G08U0F(chip#1). Due to this DNS8G08U0F goes into busy state. During this time, DNS4G08U0F(chip#2) is in ready state. So it can execute the page program command issued by the host.

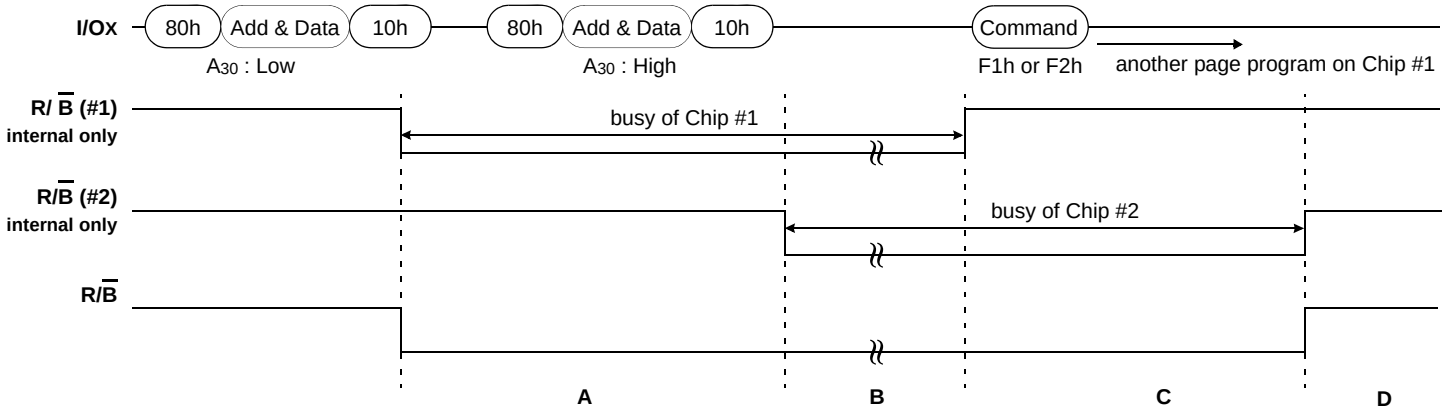
After the execution of page program by DNS4G08U0F(chip #1), it can execute another page program regardless of the DNS4G08U0F(chip #2). Before that the host needs to check the status of DNS4G08U0F(chip #1) by issuing F1h command. Only when the status of DNS4G08U0F(chip#1) becomes ready status, host can issue another page program command. If the DNS4G08U0F(chip #1) is in busy state, the host has to wait for the DNS4G08U0F(chip #1) to get into ready state.

Similarly, DNS4G08U0Fchip(chip #2) can execute another page program after the completion of the previous program. The host can monitor the status of DNS4G08U0F(chip #2) by issuing F2h command.When the DNS4G08U0F(chip #2) shows readystate, host can issue another page program command to DNS4G08U0F(chip #2).

This interleaving algorithm improves the system throughput almost twice. The host can issue page program command to each chip individually. This reduces the time lag for the completion of operation.

NOTE :
During interleave operations, 70h command is prohibited.

5.15.1 Interleave Page Program

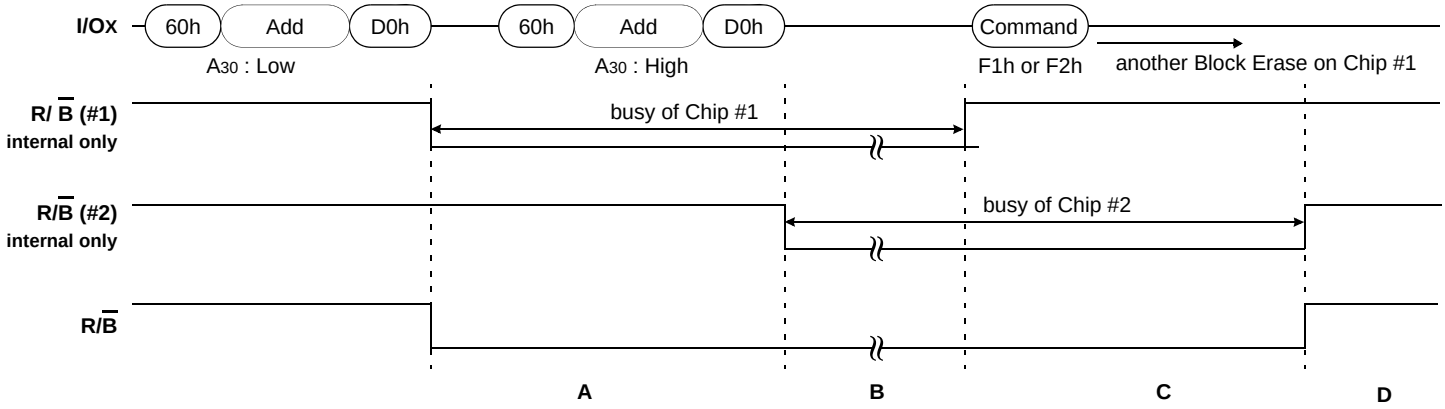


State A : Chip #1 is executing a page program operation and chip #2 is in ready state. So the host can issue a page program command to chip #2.
State B : Both chip #1 and chip #2 are executing page program operation.
State C : Page program on chip #1 is terminated, but page program on chip #2 is still operating. And the system should issue F1h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another page program command to chip #1.
State D : Chip #1 and Chip #2 are ready.

According to the above process, the system can operate page program on chip #1 and chip #2 alternately.

Status	Operation		Status Command / Data	
			F1h	F2h
A	Chip 1 : Busy,	Chip 2 : Ready	8xh	Cxh
B	Chip 1 : Busy,	Chip 2 : Busy	8xh	8xh
C	Chip 1 : Ready,	Chip 2 : Busy	Cxh	8xh
D	Chip 1 : Ready,	Chip 2 : Ready	Cxh	Cxh

5.15.2 Interleave Block Erase

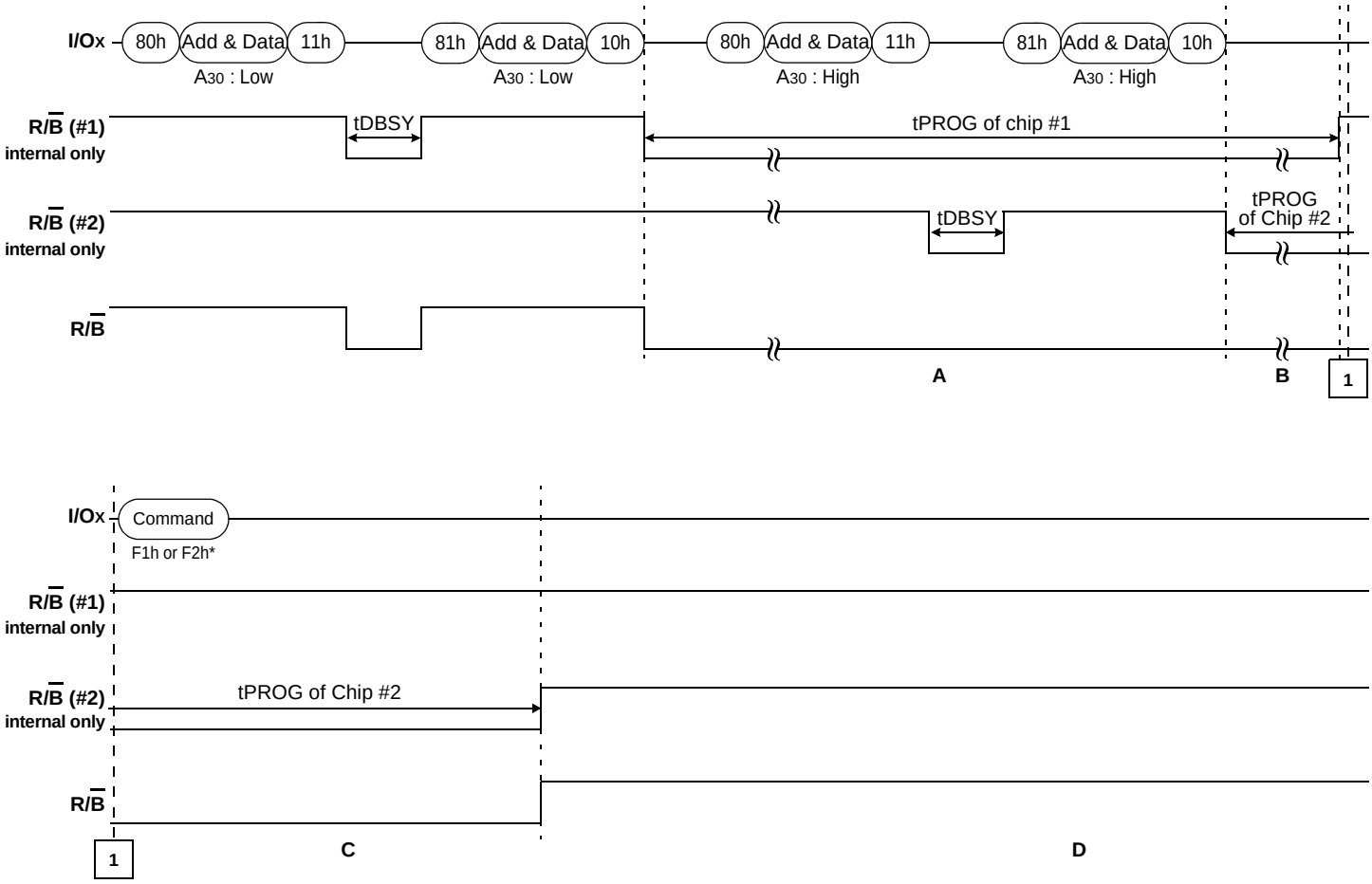


State A : Chip #1 is executing a block erase operation, and chip #2 is in ready state. So the host can issue a block erase command to chip #2.
State B : Both chip #1 and chip #2 are executing block erase operation.
State C : Block erase on chip #1 is terminated, but block erase on chip #2 is still operating. And the system should issue F1h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another block erase command to chip #1.
State D : Chip #1 and Chip #2 are ready.

According to the above process, the system can operate block erase on chip #1 and chip #2 alternately.

Status	Operation		Status Command / Data	
			F1h	F2h
A	Chip 1 : Busy,	Chip 2 : Ready	8xh	Cxh
B	Chip 1 : Busy,	Chip 2 : Busy	8xh	8xh
C	Chip 1 : Ready,	Chip 2 : Busy	Cxh	8xh
D	Chip 1 : Ready,	Chip 2 : Ready	Cxh	Cxh

5.15.3 Interleave Two-Plane Page Program

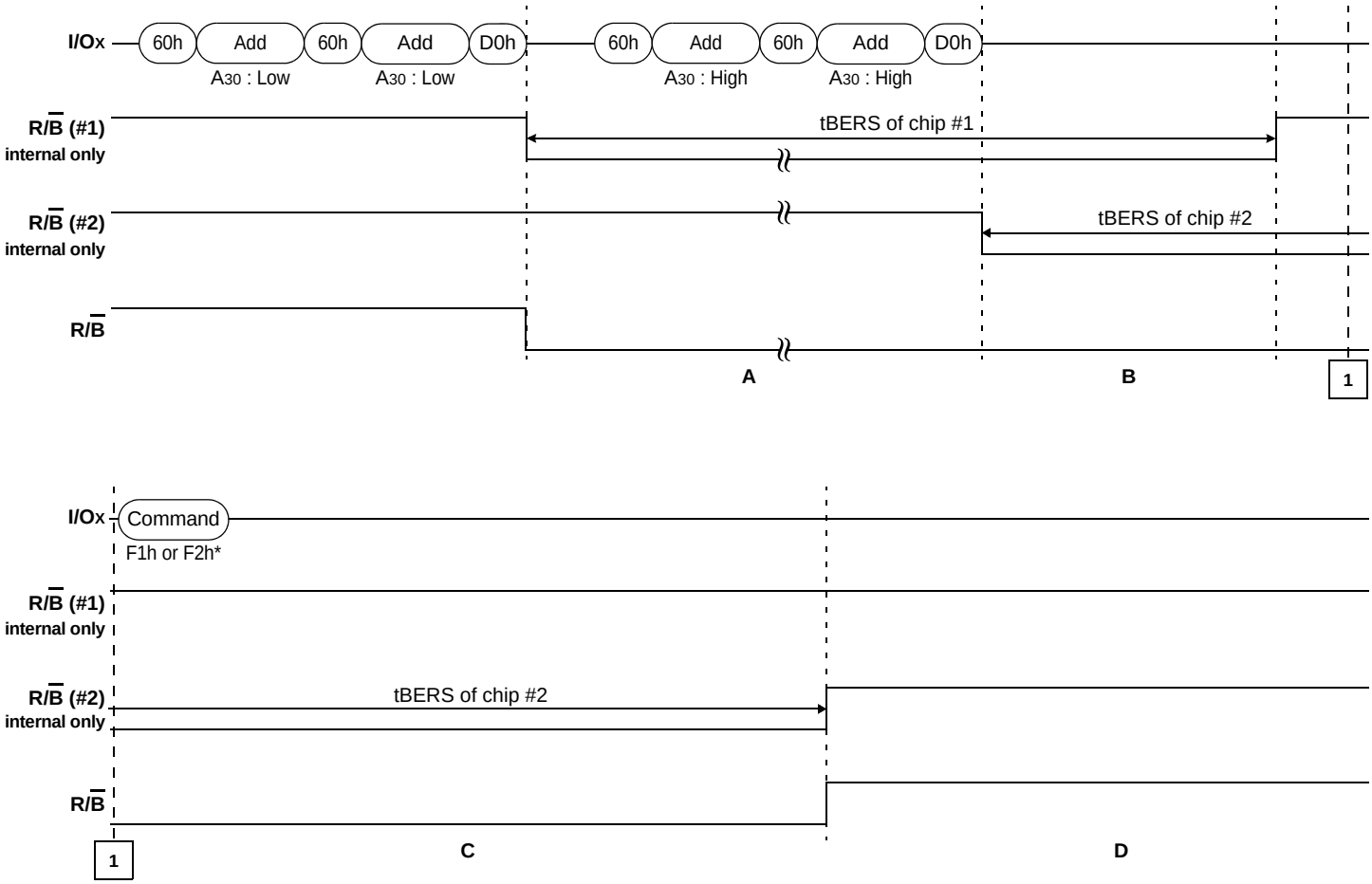


State A : Chip #1 is executing a page program operation, and chip #2 is in ready state. So the host can issue a page program command to chip #2.
State B : Both chip #1 and chip #2 are executing page program operation.
State C : Page program on chip #1 is completed and chip #1 is ready for the next operation. Chip #2 is still executing page program operation.
State D : Both chip #1 and chip #2 are ready.

NOTE :
F1h command is required to check the status of chip #1 to issue the next page program command to chip #1.
F2h command is required to check the status of chip #2 to issue the next page program command to chip #2.

According to the above process, the system can operate two-plane page program on chip #1 and chip #2 alternately.

5.15.4 Interleave Two-Plane Block Erase



State A : Chip #1 is executing a block erase operation, and chip #2 is in ready state. So the host can issue a block erase command to chip #2.
State B : Both chip #1 and chip #2 are executing block erase operation.
State C : Block erase on chip #1 is completed and chip #1 is ready for the next operation. Chip #2 is still executing block erase operation.
State D : Both chip #1 and chip #2 are ready.

NOTE :
F1h command is required to check the status of chip #1 to issue the next block erase command to chip #1.
F2h command is required to check the status of chip #2 to issue the next block erase command to chip #2.

As the above process, the system can operate two-plane block erase on chip #1 and chip #2 alternatively.

5.16 Ready/$\overline{\text{Busy}}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy), an appropriate value can be obtained with the following reference chart(Figure 23). Its value can be determined by the following guidance.

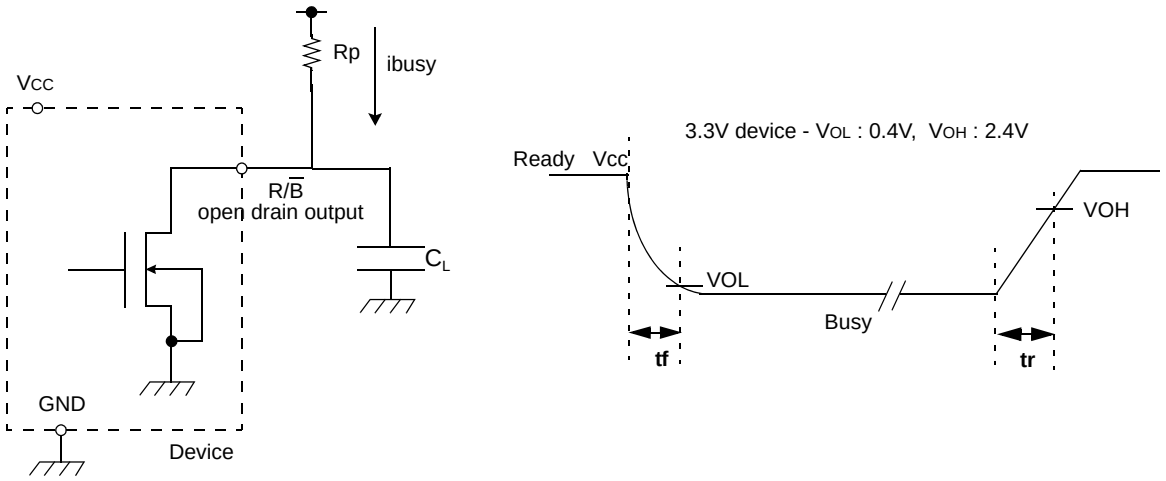
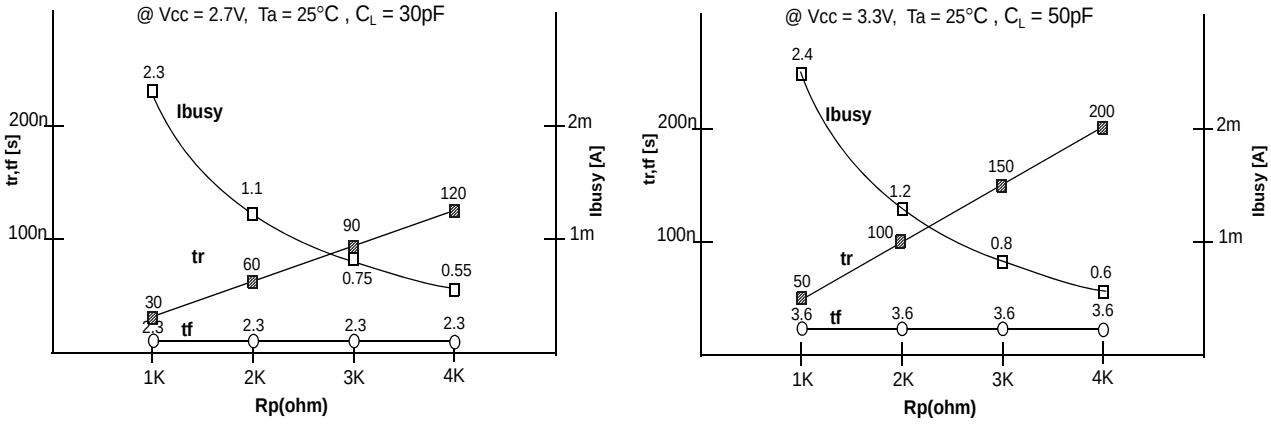


Figure 23. Rp vs tr, tf & Rp vs ibusy



Rp value guidance

$$Rp(\text{min, 3.3V part}) = \frac{V_{CC}(\text{Max.}) - V_{OL}(\text{Max.})}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr