

**D936865G28RA**  
**128M x 64 HIGH PERFORMANCE PC3 -10600**  
**UNBUFFERED DDR3 SDRAM SODIMM**

**Features**

- 240-Pin Dual In-Line Memory Module (UDIMM)
- Inputs and outputs are SSTL-15 compatible
- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock t
- Address and control signals are fully synchronous to positive clock edge
- Extended operating temperature range
- Auto Self-Refresh option
- Serial Presence Detect
- Gold contacts
- 1GB: SDRAMs are in 78-ball BGA Package
- RoHS compliance and Halogen Free

**Description**

The D936865G28RA memory module is organized as 128M x 64 bits in a 204 pin memory module. The 128M x 64 memory module uses 8 pcs 128M X8 DDR3 SDRAMs. The x64 module are ideal for use in high performance computer systems where increased memory density and fast access times are required.

**SO-DIMM Pin Description**

Pin Name	Description	Number	Pin Name	Description	Number
CK0, CK1	Clock Inputs, positive line	2	DQ0-DQ63	Data Input/Output	64
$\overline{CK0}, \overline{CK1}$	Clock Inputs, negative line	2	DM0-DM7	Data Masks/ Data strobes, Termination data strobes	8
CKE0, CKE1	Clock Enables	2	DQS0-DQS7	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS0}-\overline{DQS7}$	Data strobes complement	8
$\overline{CAS}$	Column Address Strobe	1	$\overline{RESET}$	Reset Pin	1
$\overline{WE}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
$\overline{S0}, \overline{S1}$	Chip Selects	2	$V_{DD}$	Core and I/O Power	18
A0-A9, A11, A13-A15	Address Inputs	14	$V_{SS}$	Ground	52
A10/AP	Address Input/Autoprecharge	1	$V_{REFDQ}$ $V_{REFCA}$	Input/Output Reference	2
A12/ $\overline{BC}$	Address Input/Burst chop	1	$V_{DDSPD}$	SPD and Temp sensor Power	1
BA0-BA2	SDRAM Bank Addresses	3	$V_{TT}$	Termination Voltage	2
ODT0, ODT1	On-die termination control	2	NC	Reserved for future use	3
SCL	Serial Presence Detect (SPD) Clock Input	1		Total	204
SDA	SPD Data Input/Output	1			
SA0-SA1	SPD Address	2			

\*The  $V_{DD}$  and  $V_{DDQ}$  pins are tied common to a single power-plane on these designs.

Pin Assignments

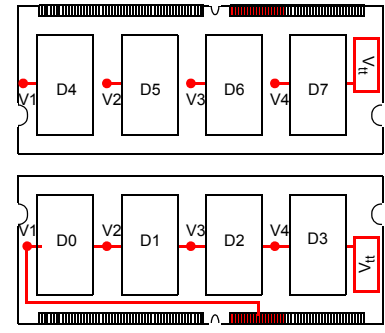
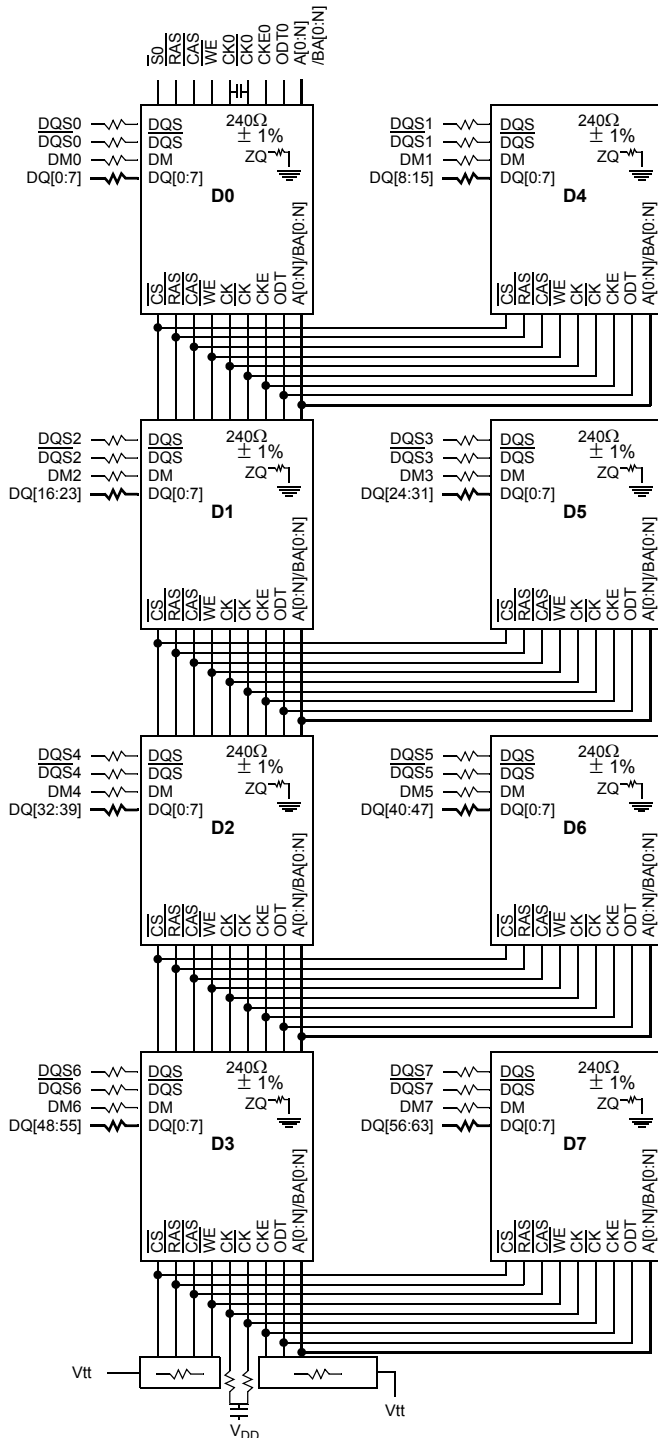
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V <sub>REFDQ</sub>	2	V <sub>SS</sub>	53	DQ19	54	V <sub>SS</sub>	105	V <sub>DD</sub>	106	V <sub>DD</sub>	157	DQ42	158	DQ46
3	V <sub>SS</sub>	4	DQ4	55	V <sub>SS</sub>	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{\text{RAS}}$	161	V <sub>SS</sub>	162	V <sub>SS</sub>
7	DQ1	8	V <sub>SS</sub>	59	DQ25	60	V <sub>SS</sub>	111	V <sub>DD</sub>	112	V <sub>DD</sub>	163	DQ48	164	DQ52
9	V <sub>SS</sub>	10	$\overline{\text{DQS0}}$	61	V <sub>SS</sub>	62	$\overline{\text{DQS3}}$	113	$\overline{\text{WE}}$	114	$\overline{\text{S0}}$	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{\text{CAS}}$	116	ODT0	167	V <sub>SS</sub>	168	V <sub>SS</sub>
13	V <sub>SS</sub>	14	V <sub>SS</sub>	65	V <sub>SS</sub>	66	V <sub>SS</sub>	117	V <sub>DD</sub>	118	V <sub>DD</sub>	169	$\overline{\text{DQS6}}$	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13 <sup>2</sup>	120	ODT1	171	DQS6	172	V <sub>SS</sub>
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{\text{S1}}$	122	NC	173	V <sub>SS</sub>	174	DQ54
19	V <sub>SS</sub>	20	V <sub>SS</sub>	71	V <sub>SS</sub>	72	V <sub>SS</sub>	123	V <sub>DD</sub>	124	V <sub>DD</sub>	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	TEST	126	V <sub>REFCA</sub>	177	DQ51	178	V <sub>SS</sub>
23	DQ9	24	DQ13	75	V <sub>DD</sub>	76	V <sub>DD</sub>	127	V <sub>SS</sub>	128	V <sub>SS</sub>	179	V <sub>SS</sub>	180	DQ60
25	V <sub>SS</sub>	26	V <sub>SS</sub>	77	NC	78	A15 <sup>2</sup>	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	$\overline{\text{DQS1}}$	28	DM1	79	BA2	80	A14 <sup>2</sup>	131	DQ33	132	DQ37	183	DQ57	184	V <sub>SS</sub>
29	DQS1	30	$\overline{\text{RESET}}$	81	V <sub>DD</sub>	82	V <sub>DD</sub>	133	V <sub>SS</sub>	134	V <sub>SS</sub>	185	V <sub>SS</sub>	186	$\overline{\text{DQS7}}$
31	V <sub>SS</sub>	32	V <sub>SS</sub>	83	A12/ $\overline{\text{BC}}$	84	A11	135	$\overline{\text{DQS4}}$	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V <sub>SS</sub>	189	V <sub>SS</sub>	190	V <sub>SS</sub>
35	DQ11	36	DQ15	87	V <sub>DD</sub>	88	V <sub>DD</sub>	139	V <sub>SS</sub>	140	DQ38	191	DQ58	192	DQ62
37	V <sub>SS</sub>	38	V <sub>SS</sub>	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V <sub>SS</sub>	195	V <sub>SS</sub>	196	V <sub>SS</sub>
41	DQ17	42	DQ21	93	V <sub>DD</sub>	94	V <sub>DD</sub>	145	V <sub>SS</sub>	146	DQ44	197	SA0	198	$\overline{\text{EVENT}}$
43	V <sub>SS</sub>	44	V <sub>SS</sub>	95	A3	96	A2	147	DQ40	148	DQ45	199	V <sub>DDSPD</sub>	200	SDA
45	$\overline{\text{DQS2}}$	46	DM2	97	A1	98	A0	149	DQ41	150	V <sub>SS</sub>	201	SA1	202	SCL
47	DQS2	48	V <sub>SS</sub>	99	V <sub>DD</sub>	100	V <sub>DD</sub>	151	V <sub>SS</sub>	152	$\overline{\text{DQS5}}$	203	V <sub>TT</sub>	204	V <sub>TT</sub>
49	V <sub>SS</sub>	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	$\overline{\text{CK0}}$	104	$\overline{\text{CK1}}$	155	V <sub>SS</sub>	156	V <sub>SS</sub>				

NC = No Connect; RFU = Reserved Future Use

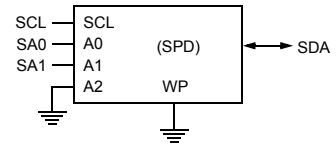
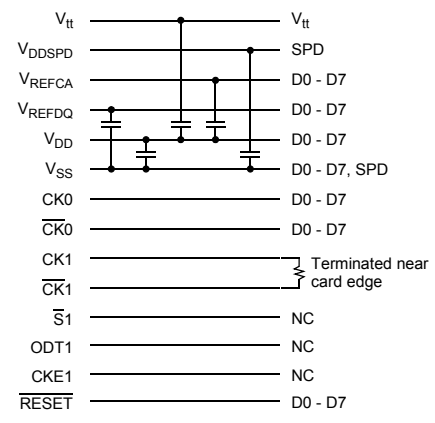
1. TEST (pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
2. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

Block Diagram

1GB, 128Mx64 Module



Address and Control Lines



Note :  
 1. DQ wiring may differ from that shown however ,DQ, DM, DQS and  $\overline{DQS}$  relationships are maintained as shown

Rank0

## Absolute Maximum Ratings

### Absolute Maximum DC Ratings

#### Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	1
T <sub>STG</sub>	Storage Temperature	-55 to +100	°C	1, 2

**Notes:**

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

### DRAM Component Operating Temperature Range

#### Temperature Range

Symbol	Parameter	Rating	Units	Notes
T <sub>OPER</sub>	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3

**Notes:**

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
  - b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Hynix DDR3 SDRAMs support Auto Self-Refresh and Extended Temperature Range and please refer to Hynix component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range.

## AC & DC Operating Conditions

### Recommended DC Operating Conditions

#### Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

## AC & DC Input Measurement Levels

### AC and DC Logic Input Levels for Single-Ended Signals

### AC and DC Input Levels for Single-Ended Command and Address Signals

#### Single Ended AC and DC Input Levels for Command and ADDRESS

Symbol	Parameter	DDR3-800/1066/1333		Unit	Notes
		Min	Max		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	V	1
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	V	1
VIH.CA(AC175)	AC input logic high	Vref + 0.175		V	1
VIL.CA(AC175)	AC input logic low	Vref - 0.175		V	1
VIH.CA(AC150)	AC Input logic high	Vref + 0.150		V	1
VIL.CA(AC150)	AC input logic low		Vref - 0.150	V	1
V <sub>RefCA(DC)</sub>	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	2, 3

Notes:

1. For input only pins except  $\overline{\text{RESET}}$ , Vref = VrefCA (DC).
2. The ac peak noise on V<sub>Ref</sub> may not allow V<sub>Ref</sub> to deviate from V<sub>RefCA(DC)</sub> by more than +/-1% VDD (for reference: approx. +/- 15 mV).
3. For reference: approx. VDD/2 +/- 15 mV.

### AC and DC Input Levels for Single-Ended Signals

DDR3 SDRAM will support two Vih/Vil AC levels for DDR3-800 and DDR3-1066 as specified in the table below.

#### Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333		Unit	Notes
		Min	Max	Min	Max		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.CA(AC175)	AC input logic high	Vref + 0.175		-	-	V	1
VIL.CA(AC175)	AC input logic low		Vref - 0.175	-	-	V	1
VIH.CA(AC150)	AC Input logic high	Vref + 0.150	Vref + 0.150			V	1
VIL.CA(AC150)	AC input logic low		Vref - 0.150		Vref - 0.150	V	1
V <sub>RefDQ(DC)</sub>	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	2,3

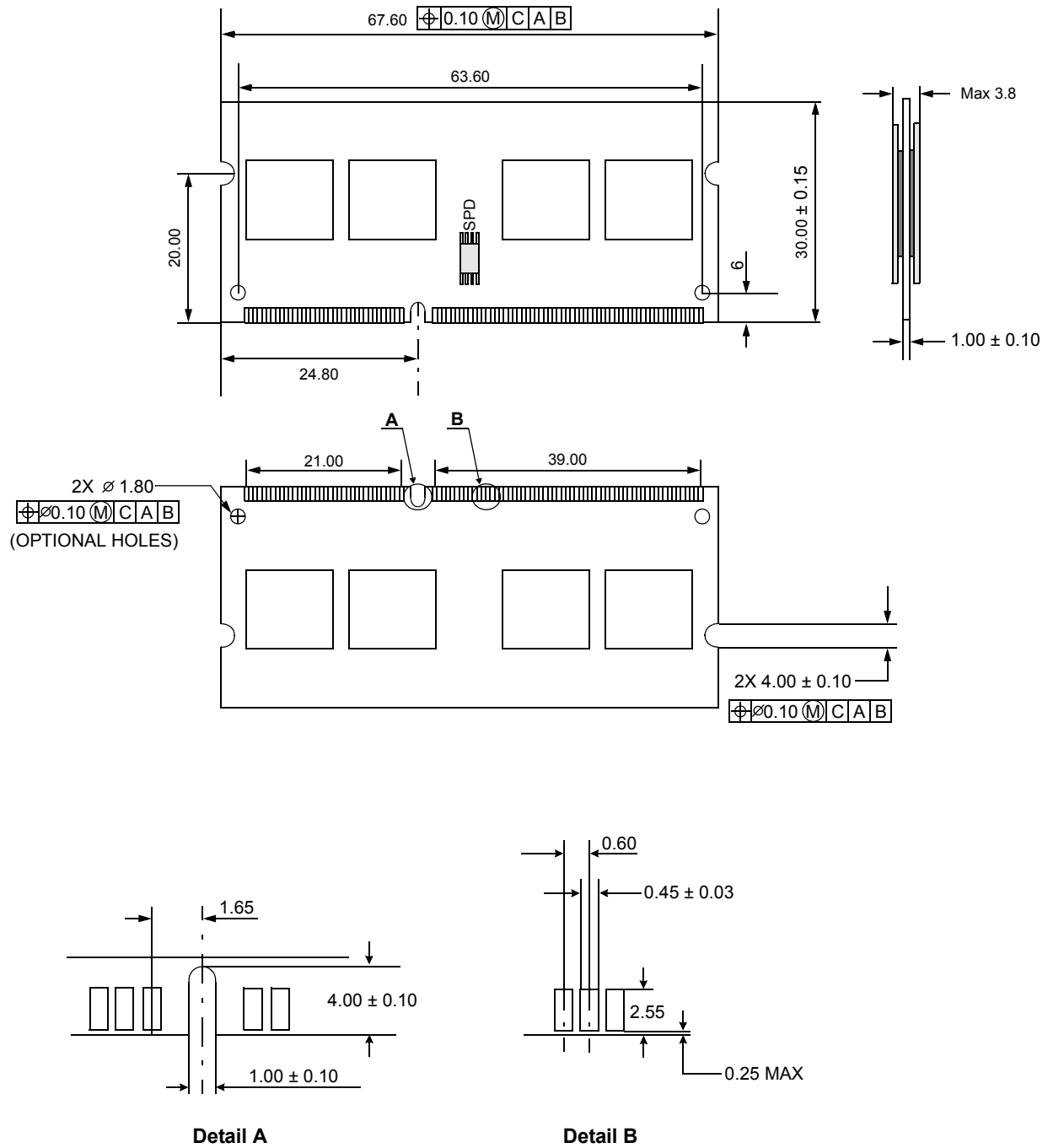
Notes:

1. Vref = VrefDQ (DC).
2. The ac peak noise on V<sub>Ref</sub> may not allow V<sub>Ref</sub> to deviate from V<sub>RefDQ(DC)</sub> by more than +/-1% VDD (for reference: approx. +/- 15 mV).
3. For reference: approx. VDD/2 +/- 15 mV.

**Package Dimension**

(1GB, 1 Ranks, 128Mx8 DDR3 SDRAMs)

Units : Millimeters



Copyright, DELSON TECHNOLOGY.

Printed in Tawan

---

The information in this document is subject to change without notice.

DELSON TECH makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of DELSON TECH.

DELSON TECH subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. DELSON TECH does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.