Delson
Technology Co, Ltd.

D73CAG04168N9

HIGH PERFORMANCE 4G bit DDR3 SDRAM

8 BANKS X 32Mbit X 16

Feature

- V_{DD} = V_{DDQ} = 1.5V ± 0.075V (JEDEC Standard Power Supply)
- 8 Internal memory banks (BA0- BA2)
- Differential clock input (CK, $\overline{CK}$)
- Programmable $\overline{CAS}$ Latency: 5, 6, 7, 8, 9, 10, 11
- $\overline{CAS}$ WRITE Latency (CWL): 5,6,7,8,9
- POSTED CAS ADDITIVE Programmable Additive Latency (AL): 0, CL-1, CL-2 clock
- Programmable Sequential / Interleave Burst Type
- Programmable Burst Length: 4, 8

  Through ZQ pin (RZQ:240 ohm±1%)
- 8n-bit prefetch architecture
- Output Driver Impedance Control
- Differential bidirectional data strobe
- Internal(self) calibration:Internal self calibration
- OCD Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- Auto Self-Refresh
- Self-Refresh Temperature
- RoHS compliance and Halogen free
- Packages:

  96-Ball BGA for x16 components

Description

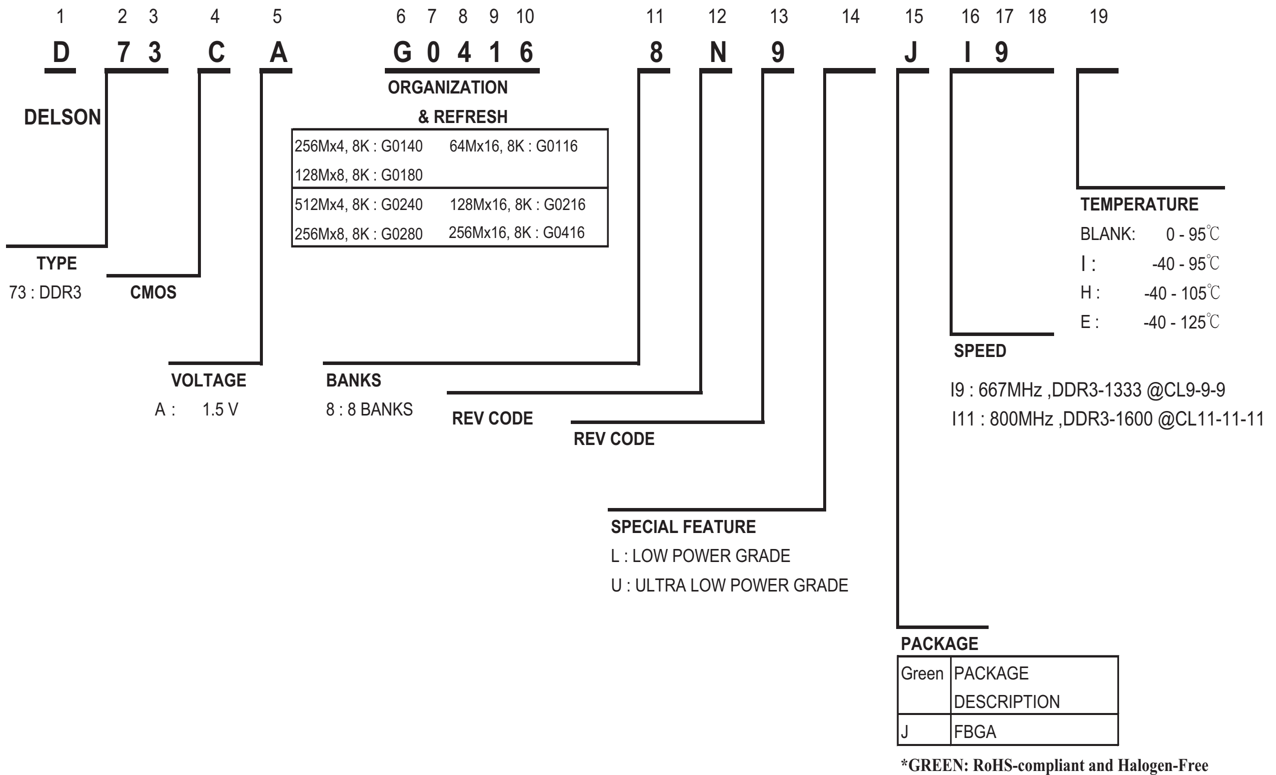
The 4Gb Double-Data-Rate-3 (DDR3) DRAMs is a high-speed CMOS Double Data Rate32 SDRAM containing 4,294,967,296 bits. It is internally configured as an octal-bank DRAM.

The 4Gb chip is organized as 128Mbit x 4 I/O x 8 bank , 64Mbit x 8 I/O x 8 banks and 32Mbit x16 I/O x 8 banks. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1600 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3 DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V power supply and are available in BGA packages.

Part Number Information



Pin Configuration – 96 balls BGA Package (x16)

< TOP View>

See the balls through the package

x 16

1	2	3		7	8	9
VDDQ	DQU5	DQU7	A	DQU4	VDDQ	VSS
VSSQ	VDD	VSS	B	$\overline{DQSU}$	DQU6	VSSQ
VDDQ	DQU3	DQU1	C	DQSU	DQU2	VDDQ
VSSQ	VDDQ	UDM	D	DQU0	VSSQ	VDD
VSS	VSSQ	DQL0	E	DML	VSSQ	VDDQ
VDDQ	DQL2	DQSL	F	DQL1	DQL3	VSSQ
VSSQ	DQL6	$\overline{DQSL}$	G	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQL4	H	DQL7	DQL5	VDDQ
NC	VSS	$\overline{RAS}$	J	CK	VSS	NC
ODT	VDD	$\overline{CAS}$	K	$\overline{CK}$	VDD	CKE
NC	$\overline{CS}$	$\overline{WE}$	L	A10/AP	ZQ	NC
VSS	BA0	BA2	M	A15	VREFCA	VSS
VDD	A3	A0	N	A12/BC#	BA1	VDD
VSS	A5	A2	P	A1	A4	VSS
VDD	A7	A9	R	A11	A6	VDD
VSS	$\overline{RESET}$	A13	T	A14	A8	VSS

Input / Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM, (DMU, DML)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS / $\overline{TQDS}$ is enabled by Mode Register A11 setting in MR1
BA0 - BA2	Input	**Bank Address Inputs:** BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 – A15	Input	**Address Inputs:** Provide the row address for Activate commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional function as below. The address inputs also provide the op-code during Mode Register Set commands.
A12 / $\overline{BC}$	Input	**Burst Chop:** A12/$\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.
DQL, DQU, DQS,($\overline{DQS}$), DQSL,($\overline{DQSL}$), DQSU,($\overline{DQSU}$),	Input/output	**Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. The data strobes DQS, DQSL, DQSU are paired with differential signals $\overline{DQS}$, $\overline{DQSL}$, $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during both reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

Symbol	Type	Function
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.5V ± 0.075V , 1.35V -0.0675V/+0.1V
V_{DD}	Supply	**Power Supply:** 1.5V ± 0.075V, 1.35V -0.0675V/+0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{SS}	Supply	**Ground**
V_{REFCA}	Supply	**Reference voltage for CA**
V_{REFDQ}	Supply	**Reference voltage for DQ**
ZQ	Supply	**Reference pin for ZQ calibration.**
Note: Input only pins (BA0-BA2, A0-A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$) do not supply termination.		

Ordering Information

Organization	Part Number	Package	Speed		
			Clock (MHz)	Data Rate (Mb/s)	CL-T_{RCD}-T_{RP}
1.5V					
256M x 16	**D73CAG04168N9JI9**	96-Ball FBGA 0.8mmx0.8mm Pitch	667	DDR3-1333	9-9-9
	D73CAG04168N9JI11		800	DDR3-1600	11-11-11

Basic Functionality

The DDR3(L) SDRAM B-Die is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3(L) SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3(L) SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3(L) SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3(L) SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

RESET and Initialization Procedure

Power-up Initialization sequence

The Following sequence is required for POWER UP and Initialization

1. Apply power ($\overline{RESET}$ is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined). $\overline{RESET}$ needs to be maintained for minimum 200µs with stable power. CKE is pulled "Low" anytime before $\overline{RESET}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD_{min} must be no greater than 200ms; and during the ramp, VDD>VDDQ and (VDD-VDDQ) <0.3 Volts.
- VDD and VDDQ are driven from a single power converter output, AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
- V_{ref} tracks VDDQ/2.

OR
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & V_{ref}.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After $\overline{RESET}$ is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clock (CK, $\overline{CK}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (t_{IS}) must be meeting. Also a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of t_{DLLK} and t_{ZQinit}.

4. The DDR3(L) DRAM will keep its on-die termination in high impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the DRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. [tXPR=max (tXS, 5tCK)]

6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1)

7. Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1)

8. Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to BA1 and BA2)

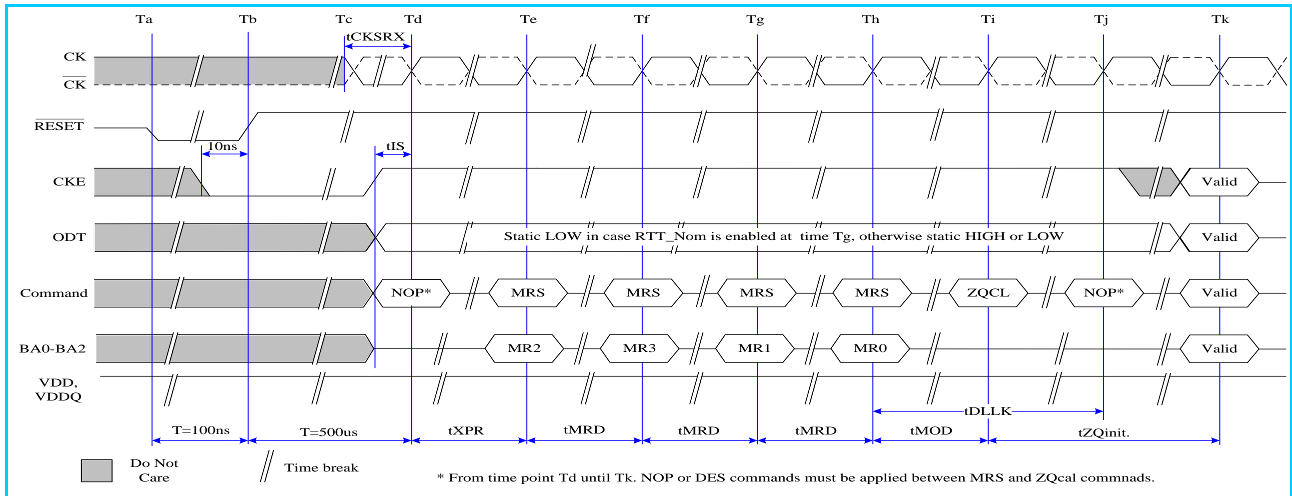
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-BA2)

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both t_{DLLK} and t_{ZQinit} completed.

12. The DDR3(L) SDRAM is now ready for normal operation.

Reset Procedure at Power Stable Condition



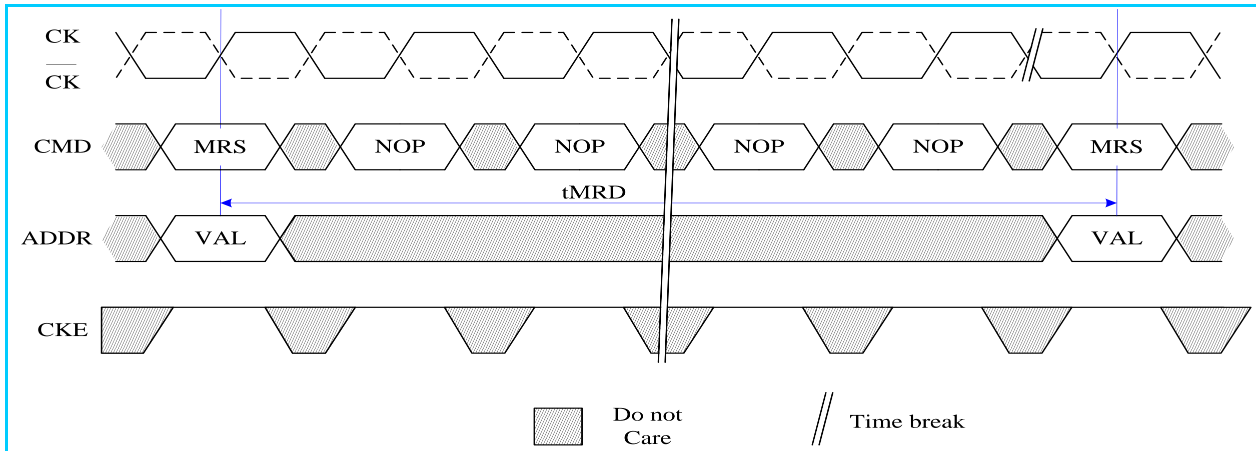
Register Definition

Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3(L) SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers ($\overline{MR}$) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents.

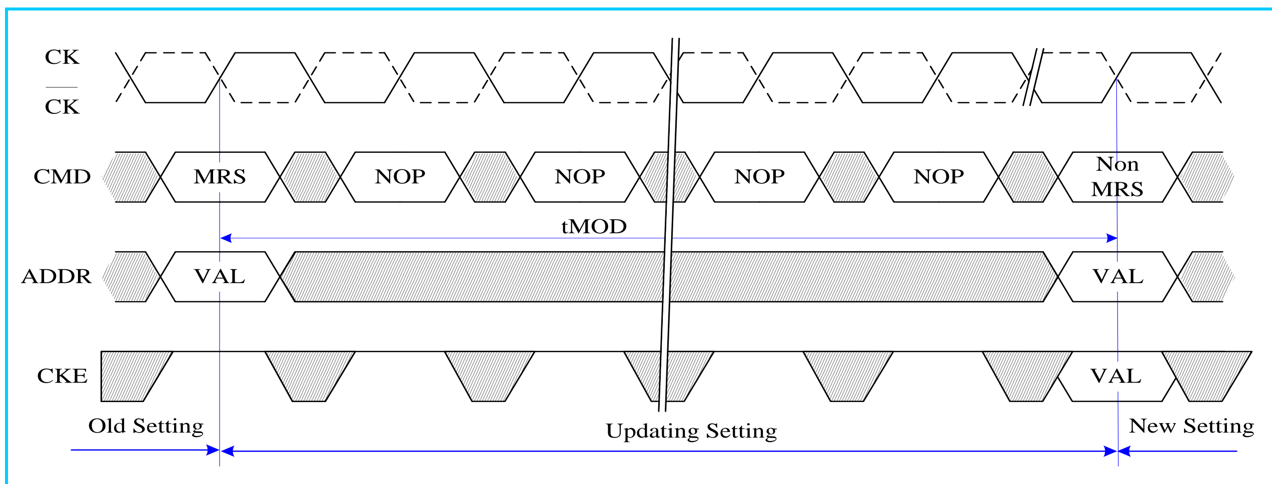
The mode register set command cycle time, t_{MRD} is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown as below.

t_{MRD} Timing



The MRS command to Non-MRS command delay, t_{MOD}, is require for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown as the following figure.

t_{MOD} Timing



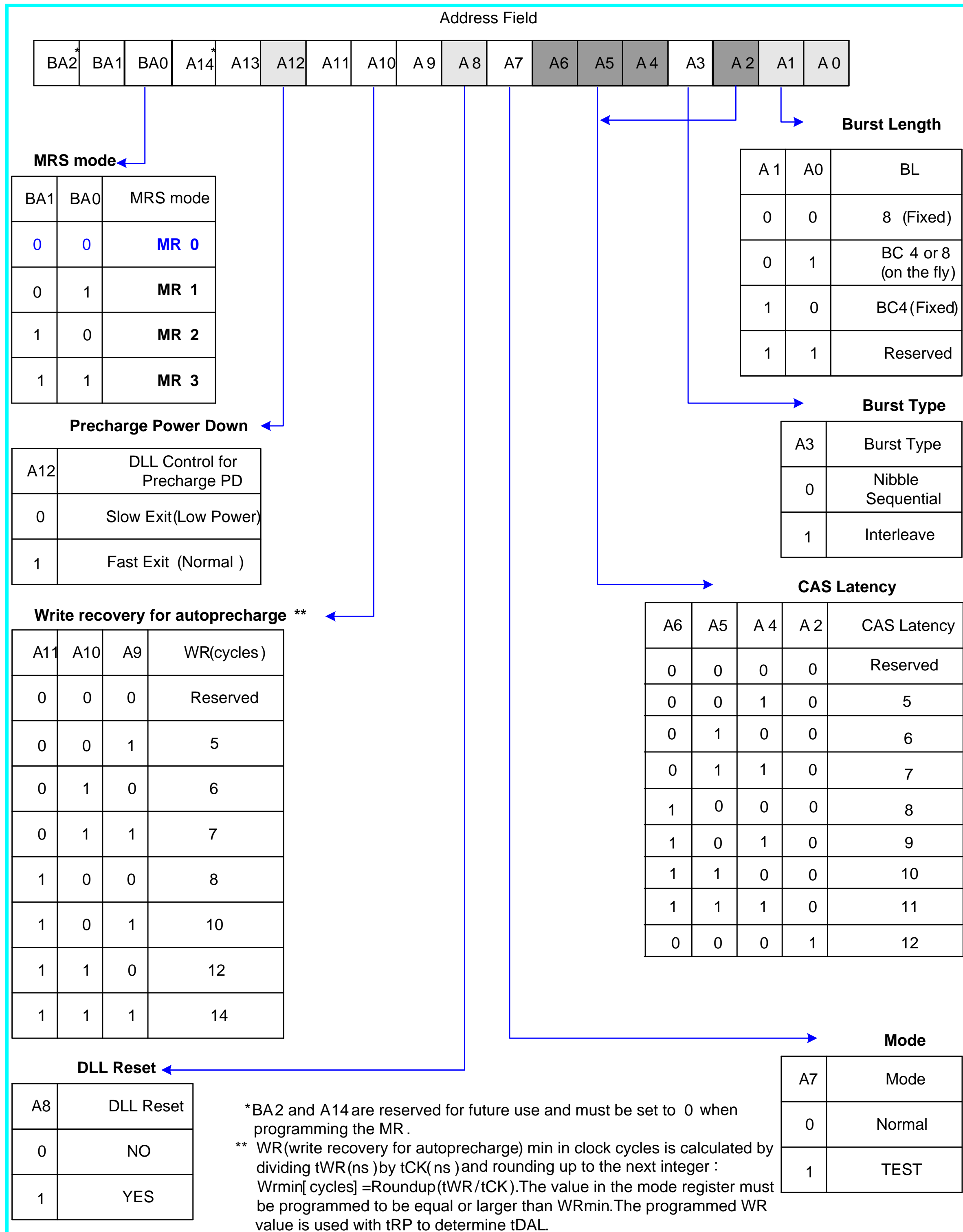
Programming the Mode Registers (Cont'd)

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

Mode Register MR0

The mode-register MR0 stores data for controlling various operating modes of DDR3(L) SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3(L) SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

MR0 Definition



MRS mode

BA1	BA0	MRS mode
0	0	MR 0
0	1	MR 1
1	0	MR 2
1	1	MR 3

Precharge Power Down

A12	DLL Control for Precharge PD
0	Slow Exit(Low Power)
1	Fast Exit (Normal)

Write recovery for autoprecharge **

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

DLL Reset

A8	DLL Reset
0	NO
1	YES

Burst Length

A1	A0	BL
0	0	8 (Fixed)
0	1	BC 4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

Burst Type

A3	Burst Type
0	Nibble Sequential
1	Interleave

CAS Latency

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12

Mode

A7	Mode
0	Normal
1	TEST

*BA2 and A14 are reserved for future use and must be set to 0 when programming the MR.

** WR(write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR(ns) by tCK(ns) and rounding up to the next integer : Wrmin[cycles] =Roundup(tWR/tCK).The value in the mode register must be programmed to be equal or larger than WRmin.The programmed WR value is used with tRP to determine tDAL.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/$\overline{BC}$.

Burst Type and Burst Order

Burst Length	Read Write	Starting Column Address (A2,A1,A0)	Burst type: Sequential (decimal) A3 = 0	Burst type: Interleaved (decimal) A3 = 1	Note
4 Chop	Read	0 , 0 , 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 , 0 , 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	
		0 , 1 , 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	
		0 , 1 , 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	
		1 , 0 , 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	
		1 , 0 , 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	
		1 , 1 , 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	
		1 , 1 , 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	
	Write	0 , V , V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1 , V , V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	
8	Read	0 , 0 , 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 , 0 , 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	
		0 , 1 , 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	
		0 , 1 , 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	
		1 , 0 , 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	
		1 , 0 , 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	
		1 , 1 , 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	
		1 , 1 , 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	
	Write	V , V , V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

Note:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/$\overline{BC}$, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

2. 0~7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.

3. T: Output driver for data and strobes are in high impedance.

4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

5. X: Do not Care.

CAS Latency

The CAS Latency is defined by MR0 (bit A9~A11) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3(L) SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0 (bit7=0) and all other bits set to the desired values shown in the MR0 definition figure. Programming bit A7 to a ‘1’ places the DDR3(L) SDRAM into a test mode that is only used by the DRAM manufacturer and should not be used. No operations or functionality is guaranteed if A7=1.

DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of ‘0’ after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

Write Recovery

The programmed WR value MR0(bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR (write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(ns) by tCK(ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal or larger than tWR (min).

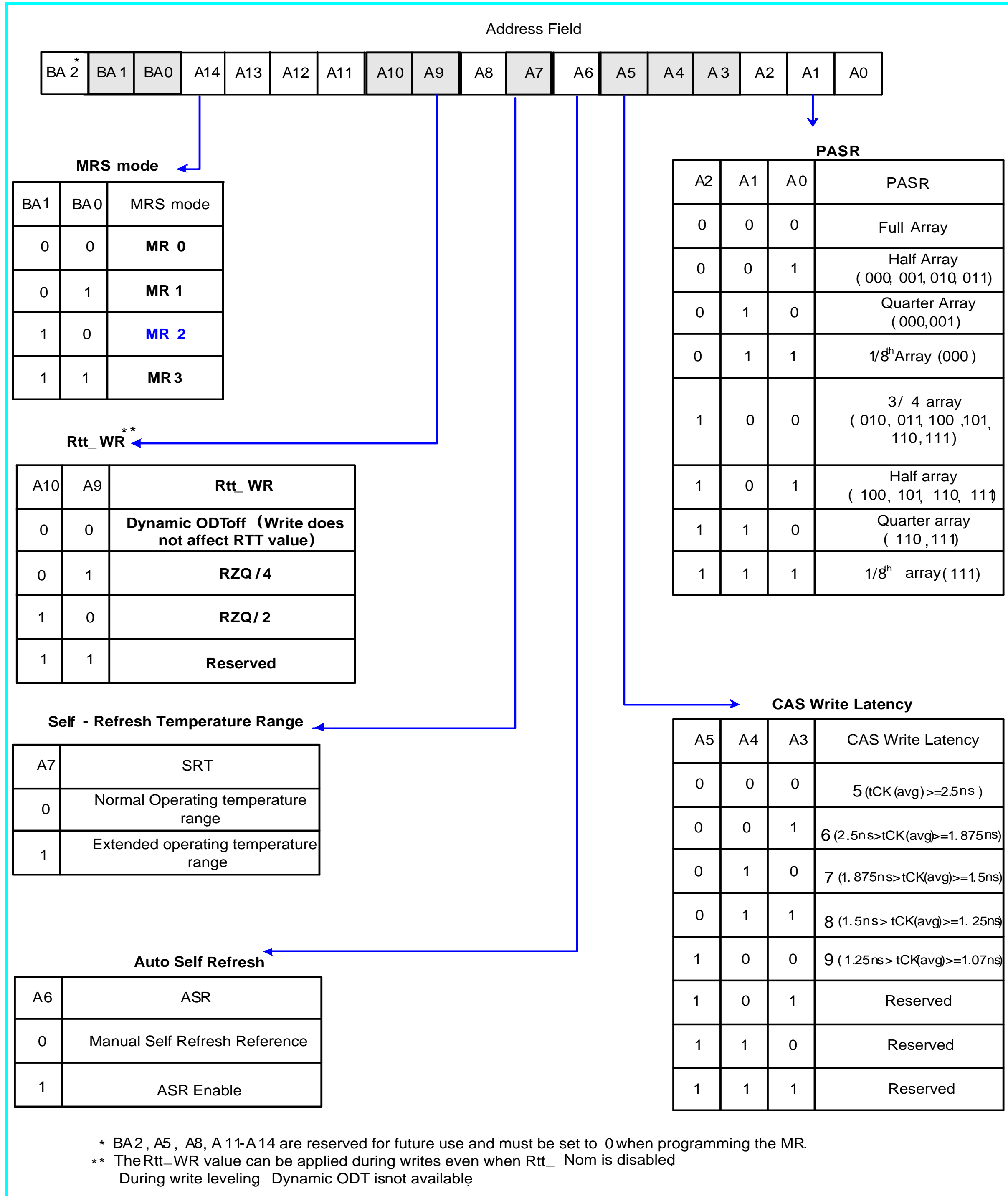
Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or ‘slow-exit’, the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or ‘fast-exit’, the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

MR2 Definition



Address Field

BA 2*	BA 1	BA0	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

MRS mode

BA1	BA0	MRS mode
0	0	MR 0
0	1	MR 1
1	0	MR 2
1	1	MR 3

Rtt_ WR**

A10	A9	Rtt_ WR
0	0	Dynamic ODToff (Write does not affect RTT value)
0	1	RZQ / 4
1	0	RZQ / 2
1	1	Reserved

Self - Refresh Temperature Range

A7	SRT
0	Normal Operating temperature range
1	Extended operating temperature range

Auto Self Refresh

A6	ASR
0	Manual Self Refresh Reference
1	ASR Enable

PASR

A2	A1	A0	PASR
0	0	0	Full Array
0	0	1	Half Array (000, 001, 010, 011)
0	1	0	Quarter Array (000,001)
0	1	1	1/8th Array (000)
1	0	0	3/ 4 array (010, 011, 100 ,101, 110, 111)
1	0	1	Half array (100, 101, 110, 111)
1	1	0	Quarter array (110 , 111)
1	1	1	1/8th array (111)

CAS Write Latency

A5	A4	A3	CAS Write Latency
0	0	0	5 (tCK (avg) >=2.5ns)
0	0	1	6 (2.5ns>tCK(avg)>=1. 875ns)
0	1	0	7 (1. 875ns>tCK(avg)>=1.5ns)
0	1	1	8 (1.5ns> tCK(avg)>=1. 25ns)
1	0	0	9 (1.25ns> tCK(avg)>=1.07ns)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

* BA2 , A5 , A8, A 11-A 14 are reserved for future use and must be set to 0 when programming the MR.
** The Rtt_WR value can be applied during writes even when Rtt_ Nom is disabled
During write leveling Dynamic ODT isnot available.

CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3(L) DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL=AL+CWL.

For more information on the supported CWL and AL settings based on the operating clock frequency, refer to “Standard Speed Bins” on page111. For detailed Write operation refer to “WRITE Operation” on page40.

Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

DDR3(L) SDRAM must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

Optional in DDR3(L) SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3(L) SDRAM devices support the following options or requirements referred to in this material. For more details refer to “Extended Temperature Usage” on page40. DDR3(L) SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

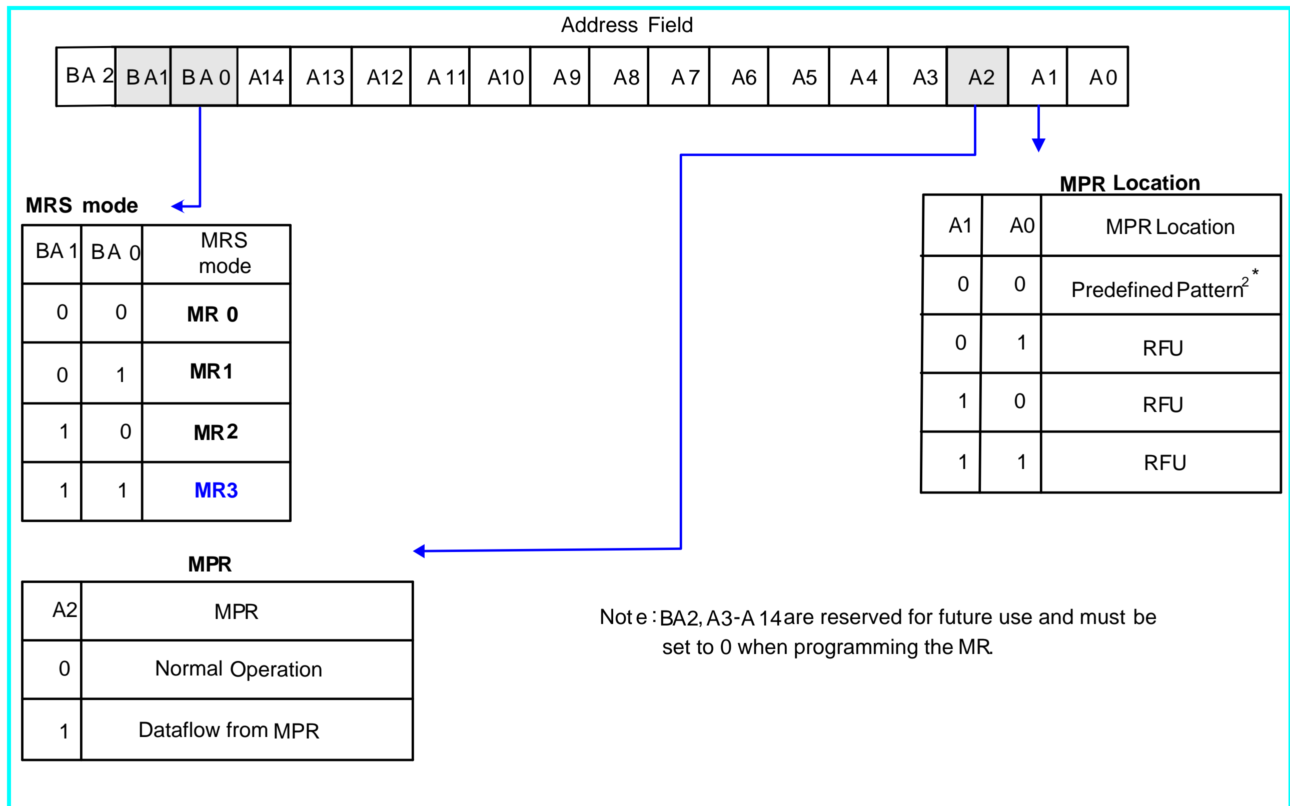
Dynamic ODT (Rtt_WR)

DDR3(L) SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3(L) SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to “Dynamic ODT” on page68.

Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

MR3 Definition

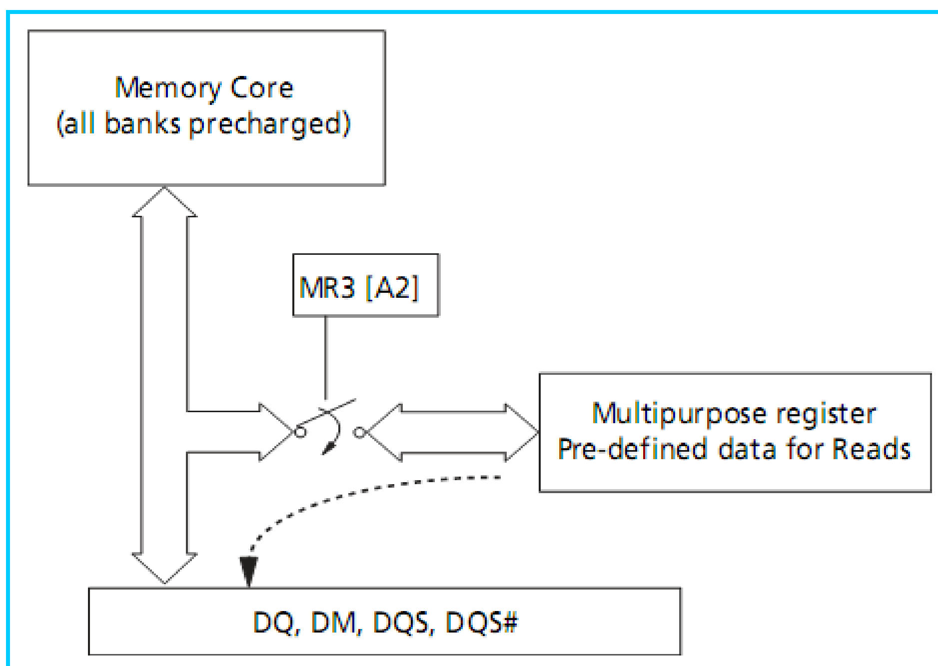


Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a Mode Register Set (MRS) command must be issued to MR3 register with bit A2=1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2=0). Power down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence.

MPR Block Diagram



To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as following Table 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown on page27. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See the page27	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

MPR Functional Description

•One bit wide logical interface via all DQ pins during READ operation.

•Register Read on x4:

•DQ[0] drives information from MPR.

•DQ[3:1] either drive the same information as DQ [0], or they drive 0b.

•Register Read on x8:

•DQL[0] and DQU[0] drive information from MPR.

•DQL[7:1] either drive the same information as DQ[0], or they drive 0b..

•Addressing during for Multi Purpose Register reads for all MPR agents:

•BA [2:0]: don't care

•A[1:0]: A[1:0] must be equal to '00'b. Data read burst order in nibble is fixed

•A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A [2]=0b, Burst order: 0,1,2,3 *)
A[2]=1b, Burst order: 4,5,6,7 *)

•A[9:3]: don't care

•A10/AP: don't care

•A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.

•A11, A13... (if available): don't care

•Regular interface functionality during register reads:

•Support two Burst Ordering which are switched with A2 and A[1:0]=00b.

•Support of read burst chop (MRS and on-the-fly via A12/BC)

•All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3(L) SDRAM.

•Regular read latencies and AC timings apply.

•DLL must be locked prior to MPR Reads.

NOTE: *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Predefined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7

NOTE: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

DDR3(L) SDRAM Command Description and Operation

Command Truth Table

Function	Abbreviation	CKE Previous Cycle	CKE Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-BA2	A13-A15	A12-$\overline{BC}$	A10-AP	A0-9, A11	NOTES
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

DDR3(L) SDRAM Command Description and Operation

Command Truth Table (Conti.)

NOTE1. All DDR3(L) SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

NOTE2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.

NOTE5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE6. The Power-Down Mode does not perform any refresh operation.

NOTE7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE8. Self Refresh Exit is asynchronous.

NOTE9. VREF (Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.

NOTE10. The No Operation command should be used in cases when the DDR3(L) SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3(L) SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.

NOTE11. The Deselect command performs the same function as No Operation command.

NOTE12. Refer to the CKE Truth Table for more detail with CKE transition.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pin relative to Vss	-0.4 ~ 1.975	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.975	V	1,3
Vin, Vout	Voltage on any pin relative to Vss	-0.4 ~ 1.975	V	1
Tstg	Storage Temperature	-55 ~ 100	°C	1,2

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.

3. VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6VDDQ, when VDD and VDDQ are less than 500Mv; Vref may be equal to or less than 300mV.

Temperature Range

Symbol	Condition	Parameter	Value	Units	Notes
Toper	Commercial	Normal Operating Temperature Range	0 to 85	°C	1,2
		Extended Temperature Range	85 to 95	°C	1,3
	Industrial	Operating Temperature Range	-40 to 95	°C	1.4

Note:

1. Operating Temperature Toper is the case surface temperature on the center/top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional apply.

a) Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1x refresh (tREFI to 7.8us) in the Extended Temperature Range.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

4. During Industrial Temperature Operation Range, the DRAM case temperature must be maintained between -40°C~95°C under all operating Conditions.

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min.	Typ.	Max.		
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3. Maximun DC value may not be great than 1.425V.The DC value is the linear average of VDD/ VDDQ(t) over a very long period of time (e.g., 1 sec).

4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.

5. Under these supply voltages, the device operates to this DDR3L specification.

6. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.

Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$ -1.5V

Slew Rate [V/ns]	tDVAC [ps] @lVIH/Ldiff(ac)l = 350Mv		tDVAC [ps] @lVIH/Ldiff(ac)l = 300mV	
	Min.	Max.	Min.	Max.
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-
1.35V				
Slew Rate [V/ns]	tDVAC [ps] @lVIH/Ldiff(ac)l = 320mV		tDVAC [ps] @lVIH/Ldiff(ac)l = 270mV	
	Min.	Max.	Min.	Max.
> 4.0	TBD	-	TBD	-
4.0	TBD	-	TBD	-
3.0	TBD	-	TBD	-
2.0	TBD	-	TBD	-
1.8	TBD	-	TBD	-
1.6	TBD	-	TBD	-
1.4	TBD	-	TBD	-
1.2	TBD	-	TBD	-
1.0	TBD	-	TBD	-
< 1.0	TBD	-	TBD	-

Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, or $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH (ac) / VIL (ac)) for ADD/CMD signals) in every half-cycle. DQS, DQSL, DQSU, $\overline{DQS}$, $\overline{DQSL}$ have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH (ac) / VIL (ac)) for DQ signals) in every half-cycle proceeding and following a valid transition. Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH150 (ac)/VIL150(ac) is used for ADD/CMD signals, then these ac-levels apply also for the singleended signals CK and $\overline{CK}$..

AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8xVDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5xVDDQ	V	
VOL(DC)	DC output low measurement level (fro IV curve linearity)	0.2xVDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT+0.1xVDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT-0.1xVDDQ	V	1

Note:

1. The swing of ±0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2.

Differential AC and DC Output Levels

Symbol	Parameter	DDR3/DDR3L	Unit	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

Note:

1. The swing of ± 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT=VDDQ/2 at each of the differential outputs.

Single Ended Output Slew Rate

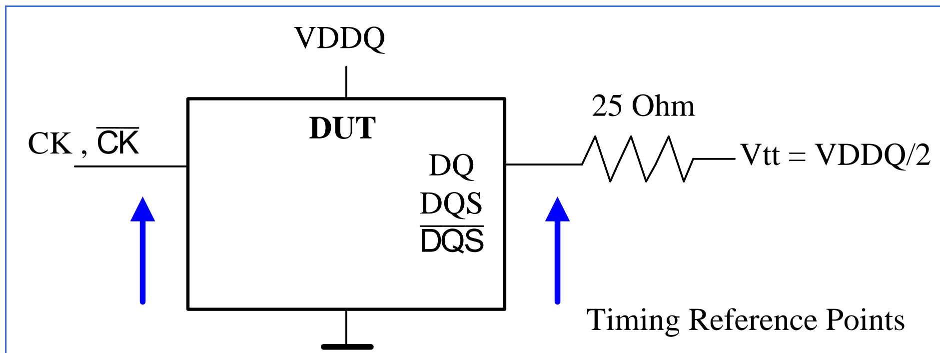
Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC)-VOL(AC)] / DeltaTRse
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC)-VOL(AC)] / DeltaTFse

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.

Reference Load for AC Timing and Output Slew Rate

The following figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



34 Ohm Output Driver DC Electrical Characteristics

A Functional representation of the output buffer is shown as below. Output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:

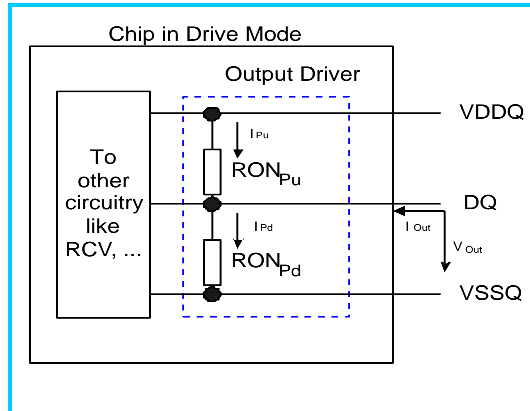
$RON_{34} = R_{ZQ} / 7$ (nominal 34.4ohms +/-10% with nominal R_{ZQ}=240ohms)

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

RON_{Pu} = [VDDQ-Vout] / I Iout I ------------------- under the condition that RON_{Pd} is turned off (1)

RON_{Pd} = Vout / I Iout I -------------------------------under the condition that RON_{Pu} is turned off (2)

Output Driver: Definition of Voltages and Currents



Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.

3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above. e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.

4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:

Measure RONPu and RONPd, but at 0.5 x VDDQ:

MM_{PuPd} = [RONPu - RONPd] / RONNom x 100

Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.

Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

Note: $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

Output Driver Sensitivity Definition

Items	Min.	Max.	Unit
RONPU@VOHdc	0.6 - dR_{ON}dTH*lDelta Tl - dR_{ON}dVH*lDelta Vl	1.1 + dR_{ON}dTH*lDelta Tl - dR_{ON}dVH*lDelta Vl	$R_{ZQ}/7$
RON@VOMdc	0.9 - dR_{ON}dTM*lDelta Tl - dR_{ON}dVM*lDelta Vl	1.1 + dR_{ON}dTM*lDelta Tl - dR_{ON}dVM*lDelta Vl	$R_{ZQ}/7$
RONPD@VOLdc	0.6 - dR_{ON}dTL*lDelta Tl - dR_{ON}dVL*lDelta Vl	1.1 + dR_{ON}dTL*lDelta Tl - dR_{ON}dVL*lDelta Vl	$R_{ZQ}/7$

Output Driver Voltage and Temperature Sensitivity

Speed Bin	DDR3(L)-1066/1333		DDR3-1600		Unit
Items	Min.	Max.	Min.	Max.	
dRONdTM	0	1.5	0	1.5	%/°C
dRONdVM	0	0.15	0	0.13	%/mV
dRONdTL	0	1.5	0	1.5	%/°C
dRONdVL	0	0.15	0	0.13	%/mV
dRONdTH	0	1.5	0	1.5	%/°C
dRONdVH	0	0.15	0	0.13	%/mV
Note: These parameters may not be subject to production test. They are verified by design and characterization.					

On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6, and A2 of the MR1 Register.

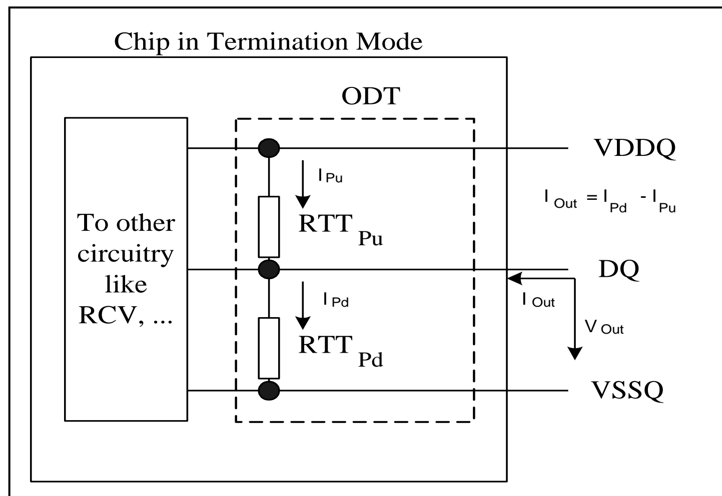
ODT is applied to the DQ, DM, DQS/$\overline{DQS}$, and TDQS/$\overline{TDQS}$ (x8 devices only) pins.

A functional representation of the on-die termination is shown in the following figure. The individual pull-up and pull-down resistors (RTT_{Pu} and RTT_{Pd}) are defined as follows:

RTT_{Pu} = [VDDQ - Vout] / I Iout I ----------------- under the condition that RTT_{Pd} is turned off (3)

RTT_{Pd} = Vout / I Iout I ----------------------------- under the condition that RTT_{Pu} is turned off (4)

On-Die Termination: Definition of Voltages and Currents



ODT DC Electrical Characteristics

The following table provides an overview of the ODT DC electrical characteristics. The values for $RTT_{60Pd120}$, $RTT_{60Pu120}$, $RTT_{120Pd240}$, $RTT_{120Pu240}$, RTT_{40Pd80}, RTT_{40Pu80}, RTT_{30Pd60}, RTT_{30Pu60}, RTT_{20Pd40}, RTT_{20Pu40} are not specification requirements, but can be used as design guide lines:

MR1 A9,A6,A2	RTT	Resistor	Vout	Min.	Nom.	Max.	Unit	Notes
1.5V								
0,1,0	120Ω	RTT120Pd240	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}	1,2,3,4
		RTT120Pu240	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}	1,2,3,4
			0.5 x VDDQ	0.9	1	1,1	R_{ZQ}	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}	1,2,3,4
		RTT120	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ} /2	1,2,5
0, 0, 1	60Ω	RTT60Pd120	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}/2	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}/2	1,2,3,4
		RTT60Pu120	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}/2	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}/2	1,2,3,4
		RTT60	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ}/4	1,2,5
0, 1, 1	40Ω	RTT40Pd80	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}/3	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}/3	1,2,3,4
		RTT40Pu80	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}/3	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}/3	1,2,3,4
		RTT40	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ}/6	1,2,5
1, 0, 1	30Ω	RTT30Pd60	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}/4	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}/4	1,2,3,4
		RTT30Pu60	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}/4	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}/4	1,2,3,4
		RTT30	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ}/8	1,2,5
1, 0, 0	20Ω	RTT20Pd40	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}/6	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}/6	1,2,3,4
		RTT20Pu40	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}/6	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}/6	1,2,3,4
		RTT20	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ}/12	1,2,5
Deviation of VM w.r.t. VDDQ/2, DVM				-5		+5	%	1,2,5,6

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.

3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration may be used to achieve the linearity spec shown above.

4. Not a specification requirement, but a design guide line.

5. Measurement definition for RTT:
Apply VIH(ac) to pin under test and measure current / (VIH(ac)), then apply VIL(ac) to pin under test and measure current / (VIL(ac)) respectively.
RTT = [VIH(ac) - VIL(ac)] / [I(VIH(ac)) - I(VIL(ac))]

6. Measurement definition for V_M and DV_M:
Measure voltage (V_M) at test pin (midpoint) with no lead:
Delta V_M = [2V_M / VDDQ -1] x 100

ODT Temperature and Voltage sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.

Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

ODT Sensitivity Definition

	Min.	Max.	Unit
RTT	0.9 - dRTTdT*lDelta Tl - dRTTdV*lDelta Vl	1.6 + dRTTdT*lDelta Tl + dRTTdV*lDelta Vl	RZQ/2,4,6,8,12

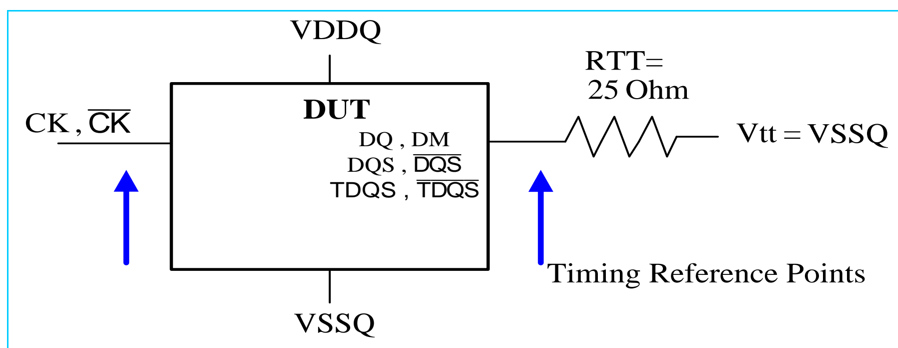
ODT Voltage and Temperature Sensitivity

	Min.	Max.	Unit
dRTTdT	0	1.5	%/°C
dRTTdV	0	0.15	%/mV
Note: These parameters may not be subject to production test. They are verified by design and characterization.			

Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in the following figure.

ODT Timing Reference Load



ODT Timing Definitions

Definitions for t_{AON}, t_{AONPD}, t_{AOF}, t_{AOFPD}, and t_{ADC} are provided in the following table and subsequent figures.

Symbol	Begin Point Definition	End Point Definition
tAON	Rising edge of CK - CK defined by the end point of ODTLon	Extrapolated point at VSSQ
tAONPD	Rising edge of CK - CK with ODT being first registered high	Extrapolated point at VSSQ
tAOF	Rising edge of CK - CK defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom
tAOFPD	Rising edge of CK - CK with ODT being first registered low	End point: Extrapolated point at VRTT_Nom
tADC	Rising edge of CK - CK defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively

IDD Specifications (1.5V)

Symbol	Parameter/Condition	DDR3-1333			DDR3-1600			Unit
		X4	X8	X16	X4	X8	X16	
IDD0	Operating Current 0 -> One Bank Activate -> Precharge	75	75	85	80	80	90	mA
IDD1	Operating Current 1 -> One Bank Activate -> Read -> Precharge	90	90	110	95	100	115	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	25	25	25	25	25	25	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	35	35	35	40	40	40	mA
IDD2Q	Precharge Quiet Standby Current	45	45	45	50	50	50	mA
IDD2N	Precharge Standby Current	50	50	50	50	50	50	mA
IDD3P	Active Power-Down Current Always Fast Exit	60	60	60	60	60	60	mA
IDD3N	Active Standby Current	60	60	73	62	62	77	mA
IDD4R	Operating Current Burst Read	155	167	240	175	187	280	mA
IDD4W	Operating Current Burst Write	135	170	240	155	193	280	mA
IDD5B	Burst Refresh Current	195	195	195	203	203	203	mA
IDD6	Self-Refresh Current: Normal Temperature Range (Tcase: 0-85°C)	25	25	25	25	25	25	mA
IDD6ET	Self-Refresh Current: Extended Temperature Range (Tcase: 0-95°C)	30	30	30	30	30	30	mA
IDD7	All Bank Interleave Read Current	250	268	300	250	280	330	mA

DDR3-1600Mbps

Speed Bin			DDR3-1600		Unit
CL-nRCD-nRP			11-11-11		
Parameter		Symbol	Min.	Max.	
Internal read command to first data		tAA	13.750 (13.125)[5,11]	20	ns
ACT to internal read or write delay time		tRCD	13.750 (13.125)[5,11]	-	ns
PRE command period		tRP	13.750 (13.125)[5,11]	-	ns
ACT to ACT or REF command period		tRC	48.750 (48.125)[5,11]	-	ns
ACT to PRE command period		tRAS	35	9*tREFI	ns
CL=5	CWL=5	tCK(AVG)	3.0	3.3	ns
	CWL=6,7,8	tCK(AVG)	Reserved	Reserved	ns
CL=6	CWL =5	tCK(AVG)	2.5	3.3	ns
	CWL =6	tCK(AVG)	Reserved	Reserved	ns
	CWL =7	tCK(AVG)	Reserved	Reserved	ns
	CWL =8	tCK(AVG)	Reserved	Reserved	ns
CL=7	CWL =5	tCK(AVG)	Reserved	Reserved	ns
	CWL =6	tCK(AVG)	1.875	<2.5	ns
	CWL =7	tCK(AVG)	Reserved	Reserved	ns
	CWL =8	tCK(AVG)	Reserved	Reserved	ns
CL=8	CWL =5	tCK(AVG)	Reserved	Reserved	ns
	CWL =6	tCK(AVG)	1.875	<2.5	ns
	CWL =7	tCK(AVG)	Reserved	Reserved	ns
	CWL =8	tCK(AVG)	Reserved	Reserved	ns
CL=9	CWL =5	tCK(AVG)	Reserved	Reserved	ns
	CWL =6	tCK(AVG)	Reserved	Reserved	ns
	CWL =7	tCK(AVG)	1.5	<1.875	ns
	CWL =8	tCK(AVG)	Reserved	Reserved	ns
CL=10	CWL =5	tCK(AVG)	Reserved	Reserved	ns
	CWL =6	tCK(AVG)	Reserved	Reserved	ns
	CWL =7	tCK(AVG)	1.5	<1.875	ns
	CWL =8	tCK(AVG)	Reserved	Reserved	ns
CL=11	CWL =5	tCK(AVG)	Reserved	Reserved	ns
	CWL =6	tCK(AVG)	Reserved	Reserved	ns
	CWL =7	tCK(AVG)	Reserved	Reserved	ns
	CWL =8	tCK(AVG)	1.250	<1.5	ns
Supported CL Settings			5,6,7,8,9,10,(11)		nCK
Supported CWL Settings			5,6,7,8		nCK

Timing Parameter by Speed Bin (DDR3-1600)

Parameter	Symbol	DDR3-1600				Units	Note
		Min.	Max.	-	-		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-			ns	
Average Clock Period	tCK(avg)	Refer to "Standard Speed Bins)				ps	
Average high pulse width	tCH(avg)	0.47	0.53	-	-	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	-	-	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max				ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	-	-	tCK(avg)	
Absolute clock LOW pulse width	tCL(abs)	0.43	-	-	-	tCK(avg)	
Clock Period Jitter	JIT(per)	-70	70	-	-	ps	
Clock Period Jitter during DLL locking period	JIT(per, lck)	-60	60	-	-	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140	140	-	-	ps	
Cycle to Cycle Period Jitter during DLL locking period	JIT(cc, lck)	120	120	-	-	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-103	103	-	-	ps	
Cumulative error across 3 cycles	tERR(3per)	-122	122	-	-	ps	
Cumulative error across 4 cycles	tERR(4per)	-136	136	-	-	ps	
Cumulative error across 5 cycles	tERR(5per)	-147	147	-	-	ps	
Cumulative error across 6 cycles	tERR(6per)	-155	155	-	-	ps	
Cumulative error across 7 cycles	tERR(7per)	-163	163	-	-	ps	
Cumulative error across 8 cycles	tERR(8per)	-169	169	-	-	ps	
Cumulative error across 9 cycles	tERR(9per)	-175	175	-	-	ps	
Cumulative error across 10 cycles	tERR(10per)	-180	180	-	-	ps	
Cumulative error across 11 cycles	tERR(11per)	-184	184	-	-	ps	
Cumulative error across 12 cycles	tERR(12per)	-188	188	-	-	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max				ps	
Data Timing							
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	100	-	-	ps	
DQ output hold time from DQS, DQS#	tQH	0.38	-	-	-	tCK(avg)	
DQ low-impedance time from CK, CK#	tLZ(DQ)	-450	225	-	-	ps	
DQ high impedance time from CK, CK#	tHZ(DQ)	-	225	-	-	ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC175/160	See Table.1 on page 124				ps	
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150/135					ps	
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100/90					ps	
DQ and DM Input pulse width for each input	tDIPW	360	-			ps	
Data Strobe Timing							
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	-	-	tCK(avg)	
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	-	-	tCK(avg)	
DQS, DQS# differential output high time	tQSH	0.4	-	-	-	tCK(avg)	
DQS, DQS# differential output low time	tQSL	0.4	-	-	-	tCK(avg)	
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	-	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	-	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-225	225	-	-	tCK(avg)	
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-450	225	-	-	tCK(avg)	
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	225	-	-	tCK(avg)	
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	-	-	tCK(avg)	
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	-	-	tCK(avg)	
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	-	-	tCK(avg)	
DQS, DQS# falling edge setup time to CK, CK#	tDSS	0.18	-	-	-	tCK(avg)	

rising edge							
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	-	-	tCK(avg)	
Command and Address Timing							
DLL locking time	tDLLK	512	-	-	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -					
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:					
WRITE recovery time	tWR	15	-	-	-	ns	
Mode Register Set command cycle time	tMRD	4	-	-	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:					
ACT to internal read or write delay time	tRCD						
PRE command period	tRP						
ACT to ACT or REF command period	tRC						
CAS# to CAS# command delay	tCCD	4	-	-	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))				nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	-	-	nCK	
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins					
ACTIVE to ACTIVE command period for 1KB page size	tRRD	tRRDmin.: max(4nCK, 6ns) tRRDmax.:					
ACTIVE to ACTIVE command period for 2KB page size	tRRD	tRRDmin.: max(4nCK, 7.5ns) tRRDmax.:					
Four activate window for 1KB page size	tFAW	30	0	-	-	ns	
Four activate window for 2KB page size	tFAW	40	0	-	-	ns	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC175/160	See on page 121				ps	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150/135					ps	
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base) DC100/90					ps	
Control and Address Input pulse width for each input	tIPW	560	-	-	-	ps	
Calibration Timing							
Power-up and RESET calibration time	tZQinit	512	-	-	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	-	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	-	-	nCK	
Reset Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -					
Self Refresh Timings							
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -					
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -				nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -					
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -					
Power Down Timings							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 6ns) tXPmax.: -		-		-	
Exit Precharge Power Down with DLL frozen to commands	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -				-	-

requiring a locked DLL							
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK ,5ns) tCKEmax.: -		-		-	
Command pass disable delay	tCPDED	tCPDEDmin.: 2 tCPDEDmin.: -				-	-
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min) tPDmax.: 9*tREFI					
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -				nCK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -				nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -				nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -				nCK	
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg))tWRPDENmax.: -				nCK	
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -				nCK	
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -				nCK	
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -					
ODT Timings							
ODT turn on Latency	ODTLon	WL-2=CWL+AL-2				nCK	
ODT turn off Latency	ODTLoff	WL-2=CWL+AL-2				nCK	
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -				nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -				nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	-	-	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	-	-	ns	
RTT turn-on	tAON	-225	225	-	-	ps	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	-	-	tCK(avg)	
RTT dynamic change skew	tADC	0.3	0.7	-	-	tCK(avg)	
Write Leveling Timings							
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	-	-	nCK	
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	-	-	nCK	
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	165	-	-	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	165	-	-	-	ps	
Write leveling output delay	tWLO	0	7.5	-	-	ns	
Write leveling output error	tWLOE	0	2	-	-	ns	

Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	245	-	195	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	245	-	195	-	ps	
Write leveling output delay	tWLO	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

Jitter Notes

Specific Note a

Unit “tCK(avg)” represents the actual tCK(avg) of the input clock under operation. Unit “nCK” represents one clock cycle of the input clock, counting the actual clock edges. ex) tMRD=4 [nCK] means; if one Mode Register Set command is registered at Tm, anther Mode Register Set command may be registered at Tm+4, even if (Tm+4-Tm) is 4 x tCK(avg) + tERR(4per), min.

Specific Note b

These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note c

These parameters are measured from a data strobe signal (DQS(L/U), $\overline{DQS(L/U)}$) crossing to its respective clock signal (CK, $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note d

These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{DQS(L/U)}$) crossing.

Specific Note e

For these parameters, the DDR3(L) SDRAM device supports tnPARAM [nCK] = RU{tPARAM[ns] / tCK(avg)[ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU{tRP/tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-1066 7-7-7, of which tRP = 13.125ns, the device will support tnRP = RU{tRP/tCK(avg)} = 7, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+7 is valid even if (Tm+7-Tm) is less than 13.125ns due to input clock jitter.

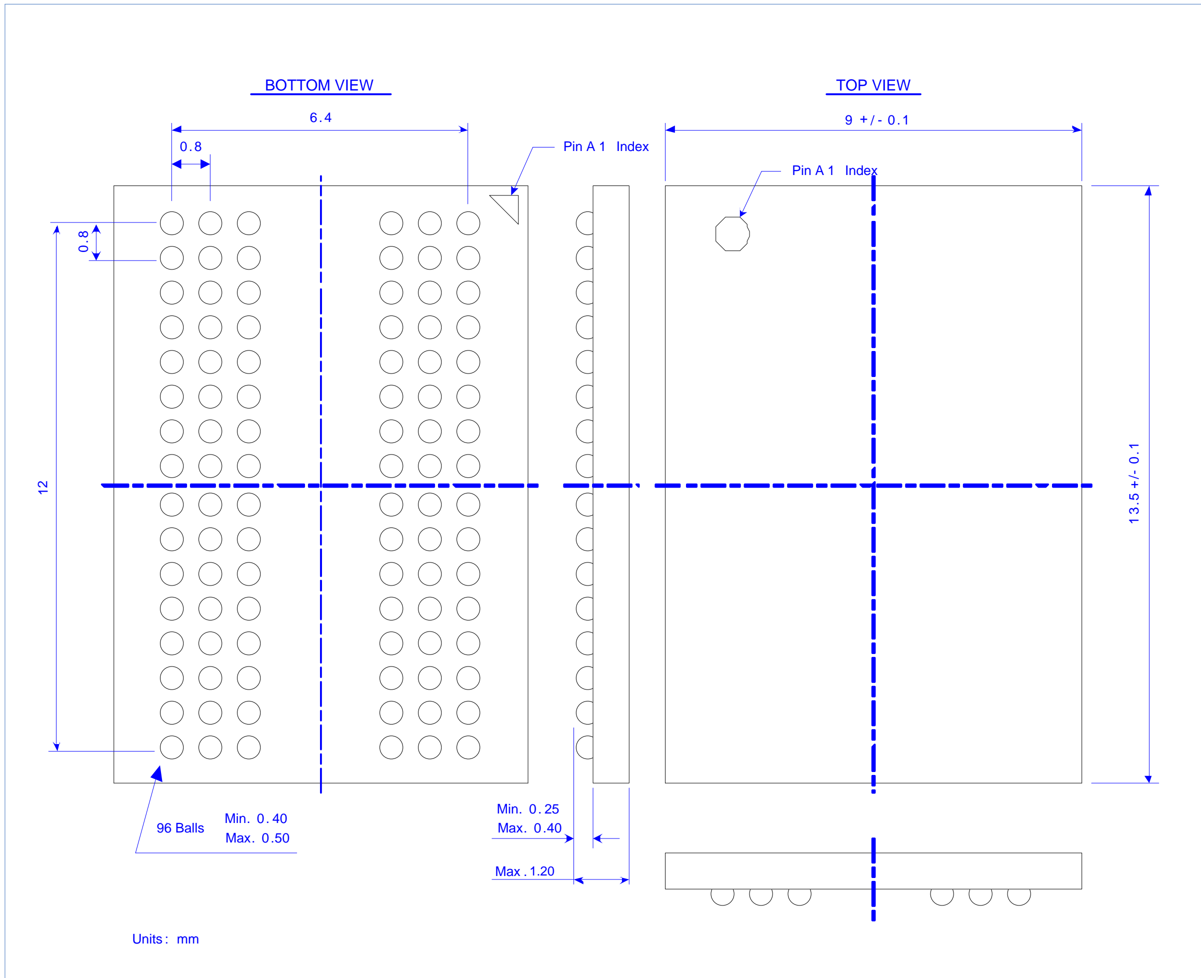
Specific Note f

When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper), act of the input clock, where 2 <= m <=12. (Output derating is relative to the SDRAM input clock.)

Specific Note g

When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (Output deratings are relative to the SDRAM input clock.)

Package Dimensions (x16; 96 balls; 0.8mmx0.8mm Pitch; FBGA)



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