Delson
Technology Co, Ltd.

D73CAG022568N9
HIGH PERFORMANCE 2G bit DDR3 SDRAM
8 BANKS X 32Mbit X 8

Feature

- 1.5V ± 0.075V / 1.35V -0.0675V/+0.1V (JEDEC Standard Power Supply)
- 8 Internal memory banks (BA0- BA2)
- Differential clock input (CK, $\overline{CK}$)
- Programmable $\overline{CAS}$ Latency: 6, 7, 8, 9, 10, 11
- Programmable Additive Latency: 0, CL-1, CL-2
- Programmable Sequential / Interleave Burst Type
- Programmable Burst Length: 4, 8
- 8 bit prefetch architecture
- Output Driver Impedance Control
- Write Leveling
- OCD Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- Auto Self-Refresh
- Self-Refresh Temperature
- RoHS compliance and Halogen free
- Packages:

78-Ball BGA for x8 components

Description

The 2Gb Double-Data-Rate-3 (DDR3) DRAMs is a high-speed CMOS Double Data Rate32 SDRAM containing 2,147,483,648 bits. It is internally configured as an octal-bank DRAM.

The 2Gb chip is organized as 32 Mbit x 8 I/O x 8 bank device. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1600 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3 DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V and 1.35V -0.0675V/+0.1V power supply and are available in BGA packages.

Pin Configuration – 78 balls BGA Package (x8)

< TOP View>

See the balls through the package

x 8

1	2	3		7	8	9
VSS	VDD	NC	A	NU/$\overline{\text{TDQS}}$	VSS	VDD
VSS	VSSQ	DQ0	B	DM/TDQS	VSSQ	VDDQ
VDDQ	DQ2	DQS	C	DQ1	DQ3	VSSQ
VSSQ	DQ6	$\overline{\text{DQS}}$	D	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4	E	DQ7	DQ5	VDDQ
NC	VSS	$\overline{\text{RAS}}$	F	CK	VSS	NC
ODT	VDD	$\overline{\text{CAS}}$	G	$\overline{\text{CK}}$	VDD	CKE
NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$	H	A10/AP	ZQ	NC
VSS	BA0	BA2	J	NC	VERFCA	VSS
VDD	A 3	A 0	K	A12/ $\overline{\text{BC}}$	BA1	VDD
VSS	A 5	A2	L	A1	A4	VSS
VDD	A7	A9	M	A11	A6	VDD
VSS	$\overline{\text{RESET}}$	A13	N	A14	A8	VSS

Input / Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM, (DMU, DML)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS / $\overline{TQDS}$ is enabled by Mode Register A11 setting in MR1
BA0 - BA2	Input	**Bank Address Inputs:** BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 – A14	Input	**Address Inputs:** Provide the row address for Activate commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional function as below. The address inputs also provide the op-code during Mode Register Set commands.
A12 / $\overline{BC}$	Input	**Burst Chop:** A12/$\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.
DQL, DQU, DQS,($\overline{DQS}$), DQSL,($\overline{DQSL}$), DQSU,($\overline{DQSU}$),	Input/output	**Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. The data strobes DQS, DQSL, DQSU are paired with differential signals $\overline{DQS}$, $\overline{DQSL}$, $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during both reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

Symbol	Type	Function
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.5V ± 0.075V , 1.35V -0.0675V/+0.1V
V_{DD}	Supply	**Power Supply:** 1.5V ± 0.075V, 1.35V -0.0675V/+0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{SS}	Supply	**Ground**
V_{REFCA}	Supply	**Reference voltage for CA**
V_{REFDQ}	Supply	**Reference voltage for DQ**
ZQ	Supply	**Reference pin for ZQ calibration.**
Note: Input only pins (BA0-BA2, A0-A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$) do not supply termination.		

Ordering Information

D73CAG022568N9

Organization	VDD	Part Number	Package	Speed		
				Clock (Mbp/s)	Data Rate (Mb/s)	CL-T_{RCD}-T_{RP}
256M x 8	1.5V	D73CAG022568N9-11	78-Ball WBGA 0.8mmx0.8mm Pitch	800	DDR3-1600	11-11-11
256M x 8	1.5V	D73CAG022568N9-9	78-Ball WBGA 0.8mmx0.8mm Pitch	667	DDR3-1333	9 -9 -9

Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A13 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BC8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

DRAM Initialization and RESET

Power-up Initialization sequence

The Following sequence is required for POWER UP and Initialization

1. Apply power ($\overline{\text{RESET}}$ is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200µs with stable power. CKE is pulled "Low" anytime before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD_{min} must be no greater than 200ms; and during the ramp, VDD>VDDQ and (VDD-VDDQ) <0.3 Volts.
- VDD and VDDQ are driven from a single power converter output, AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
- V_{ref} tracks VDDQ/2.

OR
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & V_{ref}.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clock (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (t_{IS}) must be meeting. Also a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of t_{DLLK} and t_{ZQinit}.

4. The DDR3 DRAM will keep its on-die termination in high impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the DRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. [tXPR=max(tXS, 5tCK)]

6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1)

7. Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1)

8. Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to BA1 and BA2)

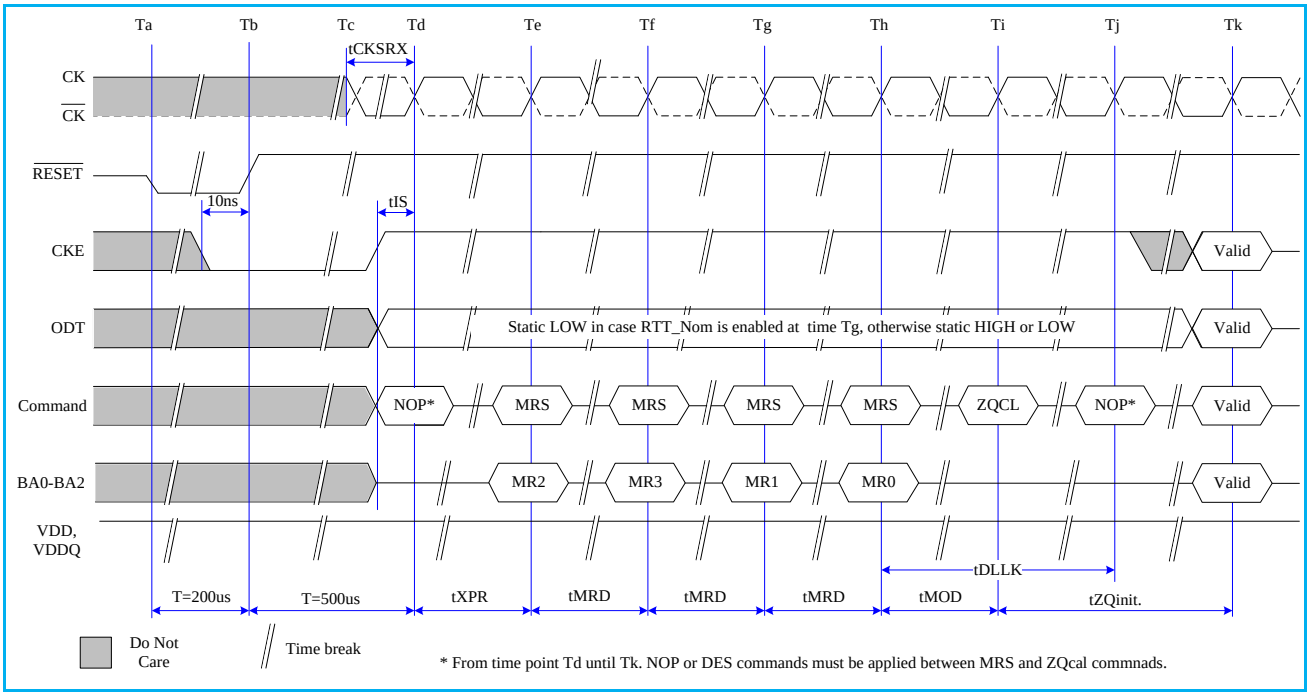
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-BA2)

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both t_{DLLK} and t_{ZQinit} completed.

12. The DDR3 SDRAM is now ready for normal operation.

DDR3 Reset and Initialization Sequence at Power-on Ramping



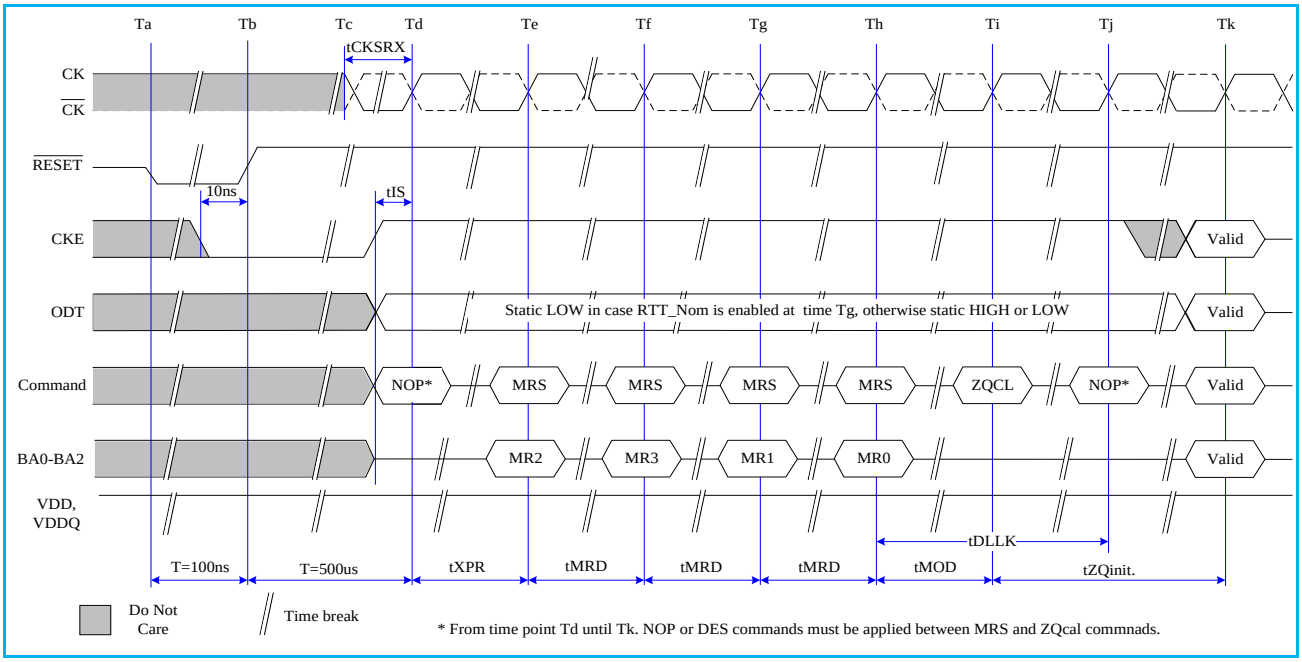
DDR3 Reset Procedure at Power Stable Condition

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2*VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100ns. CKE is pulled “Low” before RESET being de-asserted (min. time 10ns).

2. Follow Power-up Initialization Sequence step 2 to 11.

3. The Reset sequence is now completed. DDR3 SDRAM is ready for normal operation.

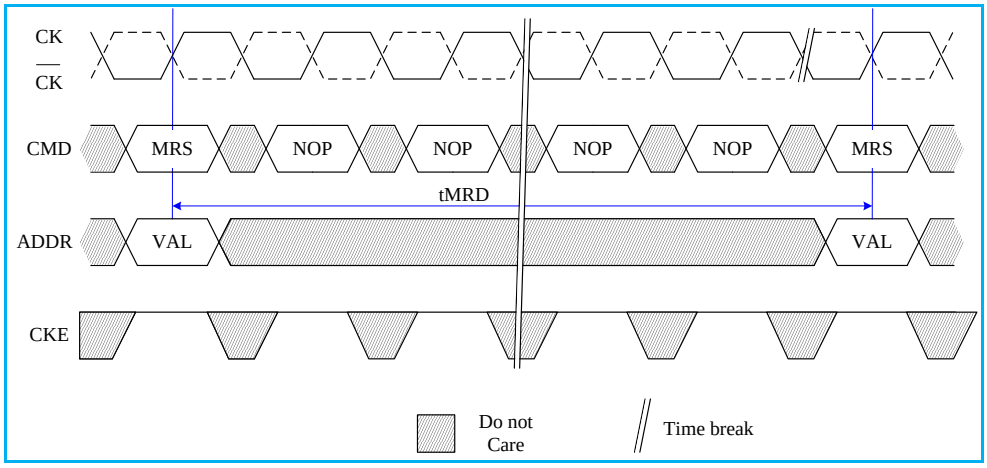


Register Definition

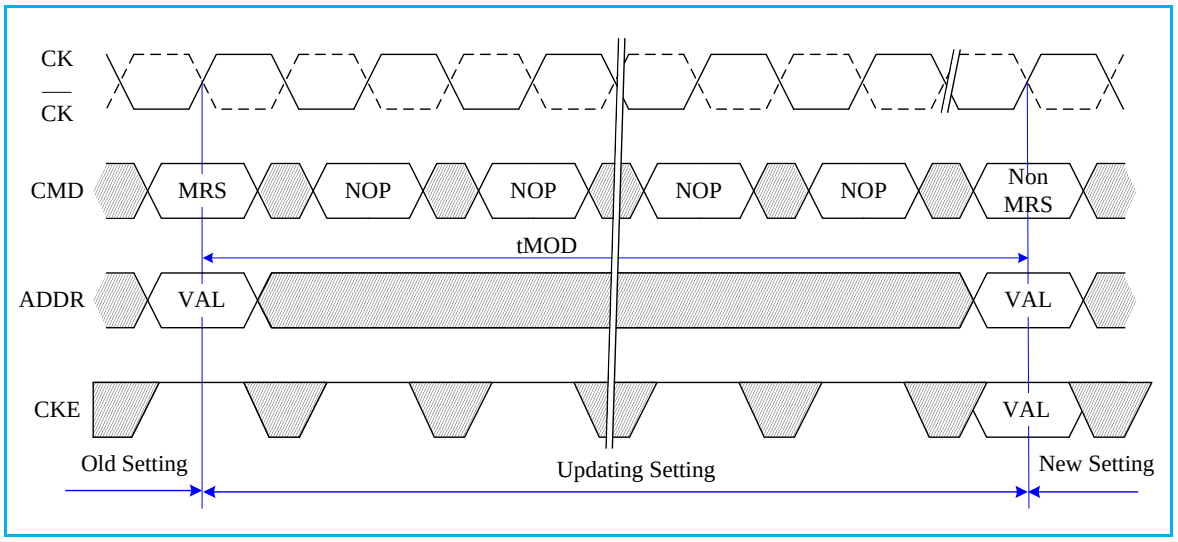
Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents

The mode register set command cycle time, t_{MRD} is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown as below.



The MRS command to Non-MRS command delay, tMOD, is require for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown as the following figure.



The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

The mode-register MR0 stores data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

MR0 Definition

Address Filed

BA2*	BA1	BA0	A13*	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

MRS mode

BA1	BA0	MRS mode
0	0	**MR0**
0	1	**MR1**
1	0	**MR2**
1	1	**MR3**

Burst Length

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

Precharge Power Down

A12	DLL Control for Precharge PD
0	Slow Exit (Low Power)
1	Fast Exit (Normal)

Burst Type

A3	Burst Type
0	Nibble Sequential
1	Interleave

Write recovery for autoprecharge**

A11	A10	A9	WR(cycles)
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

CAS Latency

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11

DLL Reset

A8	DLL Reset
0	NO
1	YES

Mode

A7	Mode
0	Normal
1	TEST

* BA2 and A13 are reserved for future use and must be set to 0 when programming the MR.
**WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer: Wrmin[cycles] = Roundup(tWR/tCK). The value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/$\overline{BC}$.

Burst Type and Burst Order

Burst Length	Read Write	Starting Column Address (A2,A1,A0)	Burst type: Sequential (decimal) A3 = 0	Burst type: Interleaved (decimal) A3 = 1	Note
4 Chop	Read	0 , 0 , 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 , 0 , 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	
		0 , 1 , 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	
		0 , 1 , 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	
		1 , 0 , 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	
		1 , 0 , 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	
		1 , 1 , 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	
		1 , 1 , 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	
	Write	0 , V , V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1 , V , V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	
8	Read	0 , 0 , 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 , 0 , 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	
		0 , 1 , 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	
		0 , 1 , 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	
		1 , 0 , 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	
		1 , 0 , 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	
		1 , 1 , 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	
		1 , 1 , 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	
	Write	V , V , V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

Note:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/$\overline{BC}$, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0~7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Do not Care.

CAS Latency

The CAS Latency is defined by MR0 (bit A9~A11) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0 (bit7=0) and all other bits set to the desired values shown in the MR0 definition figure. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should not be used. No operations or functionality is guaranteed if A7=1.

DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

Write Recovery

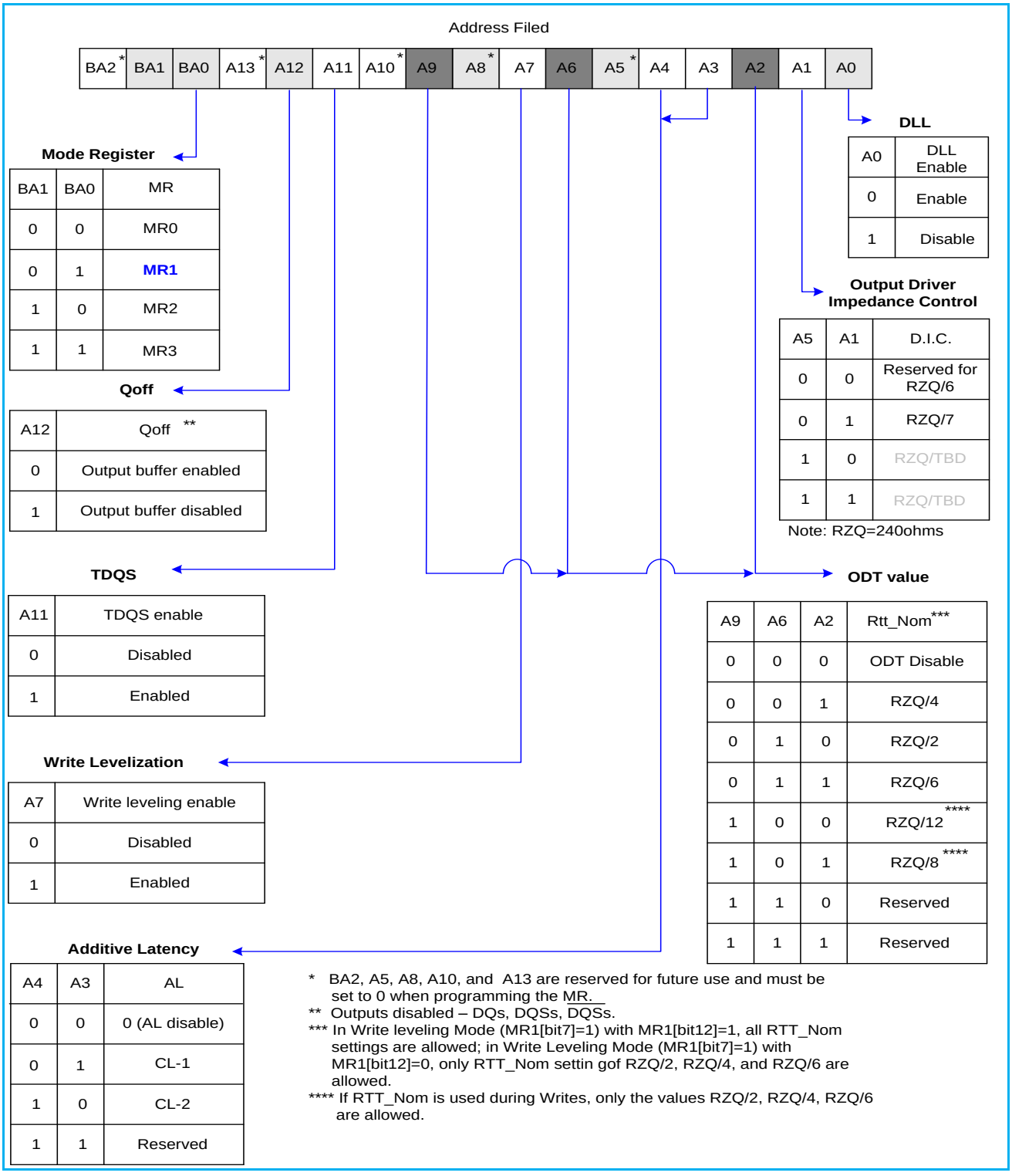
The programmed WR value MR0(bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR (write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(ns) by tCK(ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal or larger than tWR(min).

Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output strength, Rtt_Nom impedance, additive latency, WRITE leveling enable and Qoff. The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the following figure.



BA1	BA0	MR
0	0	MR0
0	1	**MR1**
1	0	MR2
1	1	MR3

A0	DLL Enable
0	Enable
1	Disable

A5	A1	D.I.C.
0	0	Reserved for RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note: RZQ=240ohms

A12	Qoff **
0	Output buffer enabled
1	Output buffer disabled

A11	TDQS enable
0	Disabled
1	Enabled

A9	A6	A2	Rtt_Nom***
0	0	0	ODT Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12****
1	0	1	RZQ/8****
1	1	0	Reserved
1	1	1	Reserved

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	AL
0	0	0 (AL disable)
0	1	CL-1
1	0	CL-2
1	1	Reserved

* BA2, A5, A8, A10, and A13 are reserved for future use and must be set to 0 when programming the MR.
** Outputs disabled – DQs, DQSs, DQSs.
*** In Write leveling Mode (MR1[bit7]=1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7]=1) with MR1[bit12]=0, only RTT_Nom settin gof RZQ/2, RZQ/4, and RZQ/6 are allowed.
**** If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4, RZQ/6 are allowed.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0=0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enable upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, expect when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation in DLL-off Mode.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10,A9}={0,0}, to disable Dynamic ODT externally.

Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1(bit A1 and A5) as shown in MR1 definition figure.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmable in MR1. A separate value (Rtt_WR) may be programmable in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown as the following table.

Additive Latency (AL) Settings

A4	A3	AL
0	0	0, (AL Disable)
0	1	CL-1
1	0	CL-2
1	1	Reserved

Write leveling

For better signal integrity, DDR3 memory module adopted fly by topology for the commands, addresses, control signals, and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate for skew.

Output Disable

The DDR3 SDRAM outputs maybe enable/disabled by MR1 (bit12) as shown in MR1 definition. When this feature is enabled (A12=1) all output pins (DQs, DQS, $\overline{DQS}$, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring modules power for example. For normal operation A12 should be set to '0'.

TDQS, $\overline{TDQS}$

TDQS (Termination Data Strobe) is a feature of x8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in x4 configurations. When enabled via the mode register, the same termination resistance function is applied to be TDQS/$\overline{TDQS}$ pins that are applied to the DQS/$\overline{DQS}$ pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the $\overline{TDQS}$ pin is not used.

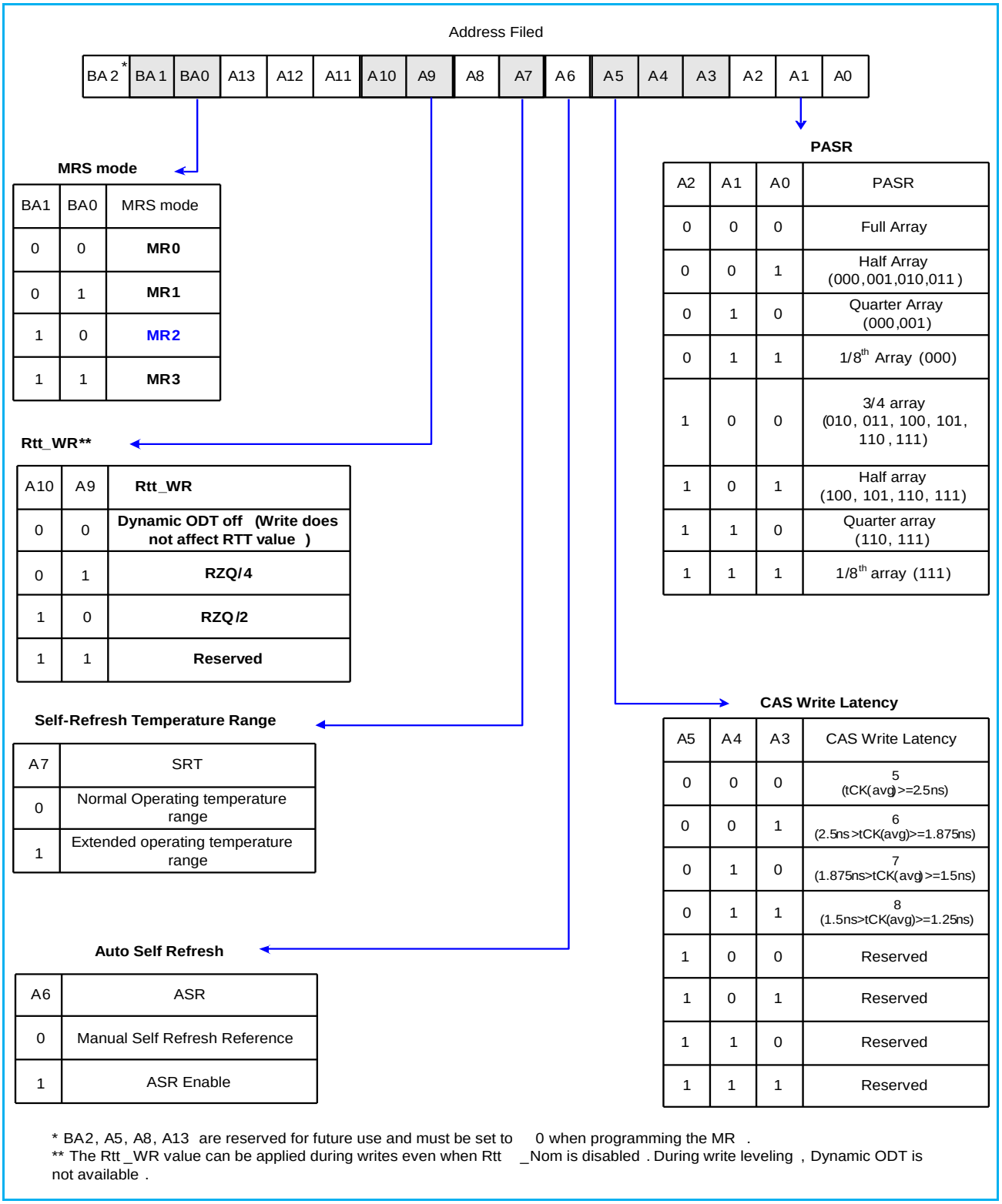
The TDQS function is available in x8 DDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for x4 configurations.

TDQS, $\overline{TDQS}$ Function Matrix

MR1 (A11)	DM / TDQS	NU / TDQS
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	TDQS
Note:		
1. If TDQS is enabled, the DM function is disabled.		
2. When not used, TDQS function can be disabled to save termination power.		
3. TDQS function is only available for x8 DRAM and must be disabled for x4		

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.



BA1	BA0	MRS mode
0	0	**MR0**
0	1	**MR1**
1	0	**MR2**
1	1	**MR3**

A10	A9	Rtt_WR
0	0	**Dynamic ODT off (Write does not affect RTT value)**
0	1	**RZQ/4**
1	0	**RZQ/2**
1	1	**Reserved**

A7	SRT
0	Normal Operating temperature range
1	Extended operating temperature range

A6	ASR
0	Manual Self Refresh Reference
1	ASR Enable

A2	A1	A0	PASR
0	0	0	Full Array
0	0	1	Half Array (000,001,010,011)
0	1	0	Quarter Array (000,001)
0	1	1	1/8th Array (000)
1	0	0	3/4 array (010, 011, 100, 101, 110 , 111)
1	0	1	Half array (100, 101, 110, 111)
1	1	0	Quarter array (110, 111)
1	1	1	1/8th array (111)

A5	A4	A3	CAS Write Latency
0	0	0	5 (tCK(avg)>=2.5ns)
0	0	1	6 (2.5ns>tCK(avg)>=1.875ns)
0	1	0	7 (1.875ns>tCK(avg)>=1.5ns)
0	1	1	8 (1.5ns>tCK(avg)>=1.25ns)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

* BA2, A5, A8, A13 are reserved for future use and must be set to 0 when programming the MR .
** The Rtt _WR value can be applied during writes even when Rtt _Nom is disabled . During write leveling , Dynamic ODT is not available .

CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL=AL+CWL.

Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

DDR3 SDRAM must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

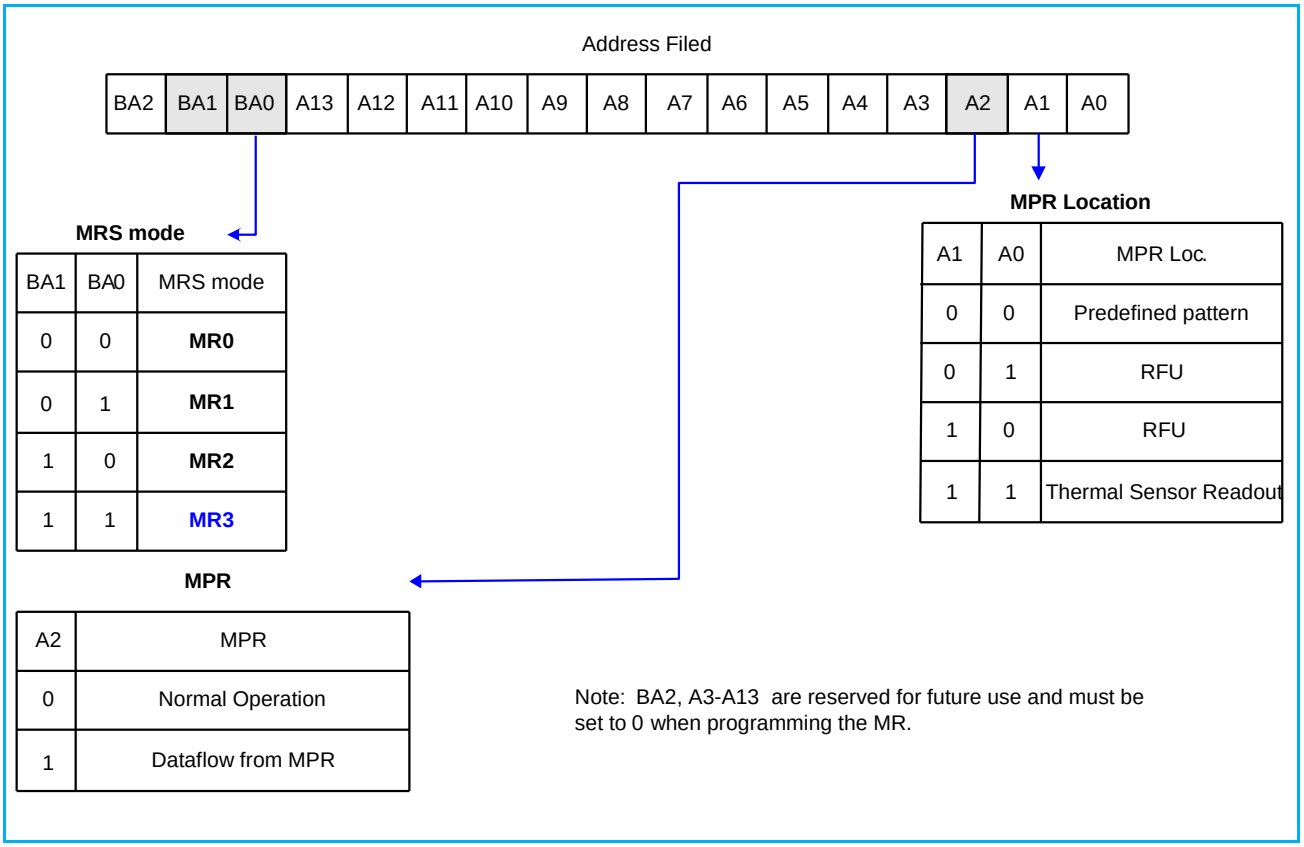
Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to “Extended Temperature Usage” on page48. DDR3 SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available.

Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



BA1	BA0	MRS mode
0	0	**MR0**
0	1	**MR1**
1	0	**MR2**
1	1	**MR3**

A1	A0	MPR Loc.
0	0	Predefined pattern
0	1	RFU
1	0	RFU
1	1	Thermal Sensor Readout

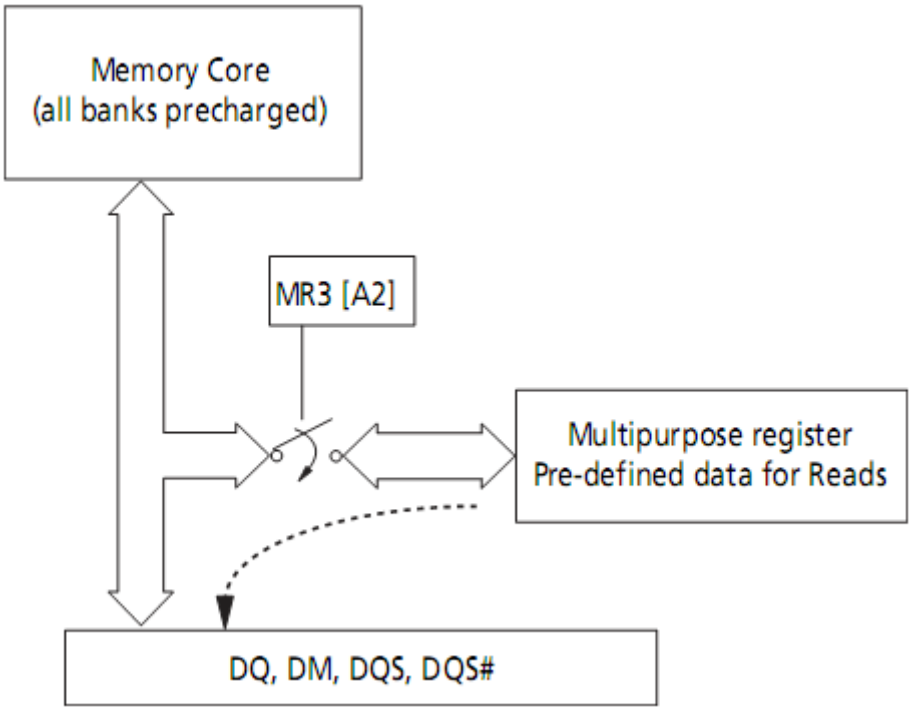
A2	MPR
0	Normal Operation
1	Dataflow from MPR

Note: BA2, A3-A13 are reserved for future use and must be set to 0 when programming the MR.

Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a Mode Register Set (MRS) command must be issued to MR3 register with bit A2=1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2=0). Power down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure20.



To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table12. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table13. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See Table 13	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

MPR Functional Description

•One bit wide logical interface via all DQ pins during READ operation.

•Register Read on x4:

•DQ[0] drives information from MPR.

•DQ[3:1] either drive the same information as DQ[0], or they drive 0b.

•Register Read on x8:

•DQ[0] drives information from MPR.

•DQ[7:1] either drive the same information as DQ[0], or they drive 0b.

•Register Read on x16:

•DQL[0] and DQU[0] drive information from MPR.

•DQL[7:1] and DQU[7:1] either drive the same information as DQL[0], or they drive 0b.

•Addressing during for Multi Purpose Register reads for all MPR agents:

•BA[2:0]: don't care

•A[1:0]: A[1:0] must be equal to '00'b. Data read burst order in nibble is fixed

•A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3 *)

A[2]=1b, Burst order: 4,5,6,7 *)

•A[9:3]: don't care

•A10/AP: don't care

•A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.

•A11, A13,... (if available): don't care

•Regular interface functionality during register reads:

•Support two Burst Ordering which are switched with A2 and A[1:0]=00b.

•Support of read burst chop (MRS and on-the-fly via A12/BC)

•All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.

•Regular read latencies and AC timings apply.

•DLL must be locked prior to MPR Reads.

NOTE: *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

DDR3 SDRAM Command Description and Operation

Command Truth Table

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{BA0}$	A13	A12	A10	A0-9	NOTE
		Previous Cycle	Current Cycle					$\overline{BA2}$	A15	$\overline{BC}$	AP	A11	
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	
				H	X	X	X	X	X	X	X	X	
Self Refresh Exit	SRX	L	H	L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

DDR3 SDRAM Command Description and Operation

Command Truth Table (Conti.)

NOTE1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

NOTE2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.

NOTE5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE6. The Power-Down Mode does not perform any refresh operation.

NOTE7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE8. Self Refresh Exit is asynchronous.

NOTE9. VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.

NOTE10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.

NOTE11. The Deselect command performs the same function as No Operation command.

NOTE12. Refer to the CKE Truth Table for more detail with CKE transition.

CKE Truth Table

Current State	CKE		Command (N)	Action (N)	Notes
	Previous Cycle (N-1)	Current Cycle (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power-Down	L	L	X	Maintain Power-Down	
	L	H	DESELECT or NOP	Power-Down Exit	
Self-Refresh	L	L	X	Maintain Self-Refresh	
	L	H	DESELECT or NOP	Self-Refresh Exit	
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	
Reading	H	L	DESELECT or NOP	Power-Down Entry	
Writing	H	L	DESELECT or NOP	Power-Down Entry	
Precharging	H	L	DESELECT or NOP	Power-Down Entry	
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	
	H	L	REFRESH	Self-Refresh	

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registrations. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh modes can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are NOP and DESELECT only.

NOTE 13 Self-Refresh cannot be entered during Read or Write operations.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15“X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

NOTE 18‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.)

as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

No Operation (NOP) Command

The No operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP ($\overline{CS}$ low and $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Deselect Command

The Deselect function ($\overline{CS}$ HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operations until A0 bit set back to “0”. The MR1 A0 bit for DLL control can be switched either during initialization or later.

The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

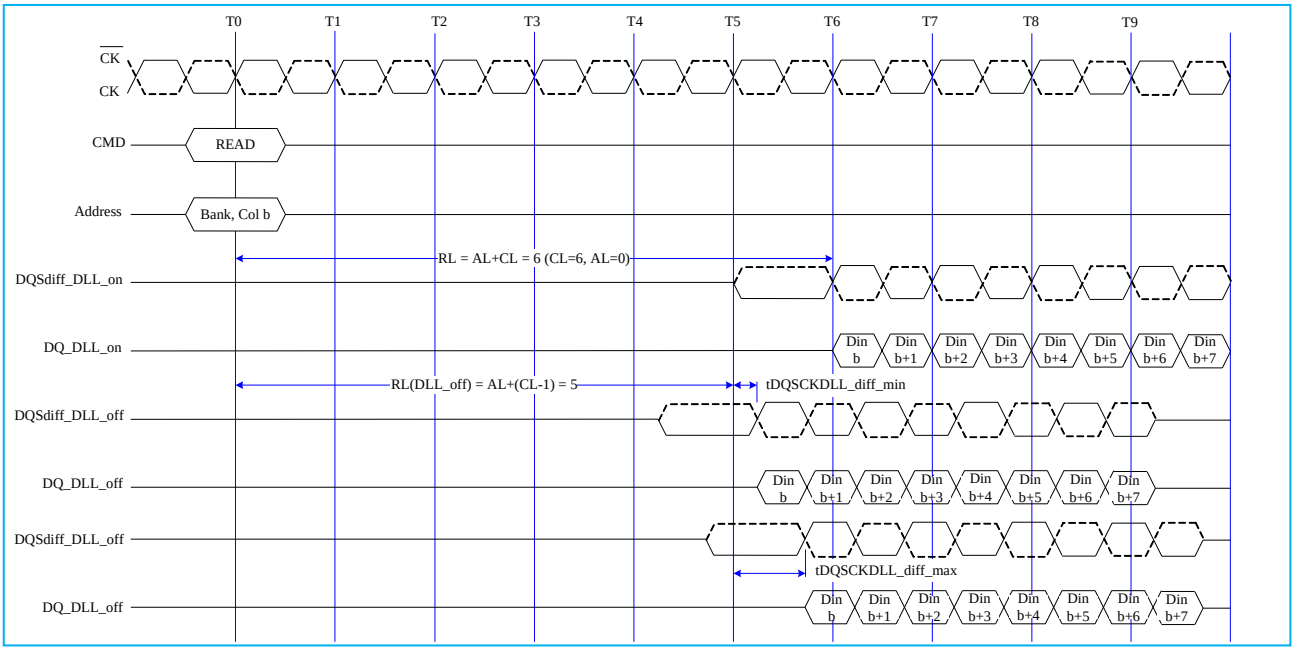
Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK) but not the data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL-1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation have shown at the following Timing Diagram (CL=6, BL=8)

DLL-off mode READ Timing Operation



Note: The tDQSCK is used here for DQS, DQS, and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ, DQS, and $\overline{DQS}$ signals will still be tDQSQ.

DLL on/off switching procedure

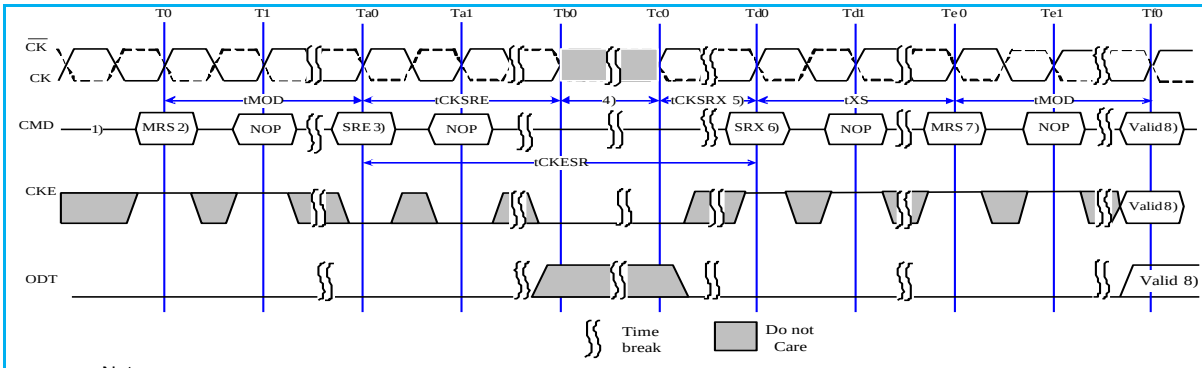
DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operation until A0 bit set back to “0”.

DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during Self-Refresh outlined in the following procedure:

1. Starting from Idle state (all banks pre-charged, all timing fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL).
2. Set MR1 Bit A0 to “1” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) satisfied.
5. Change frequency, in guidance with “Input Clock Frequency Change” section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, and then set Mode Registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, and then DRAM is ready for next command.

DLL Switch Sequence from DLL-on to DLL-off

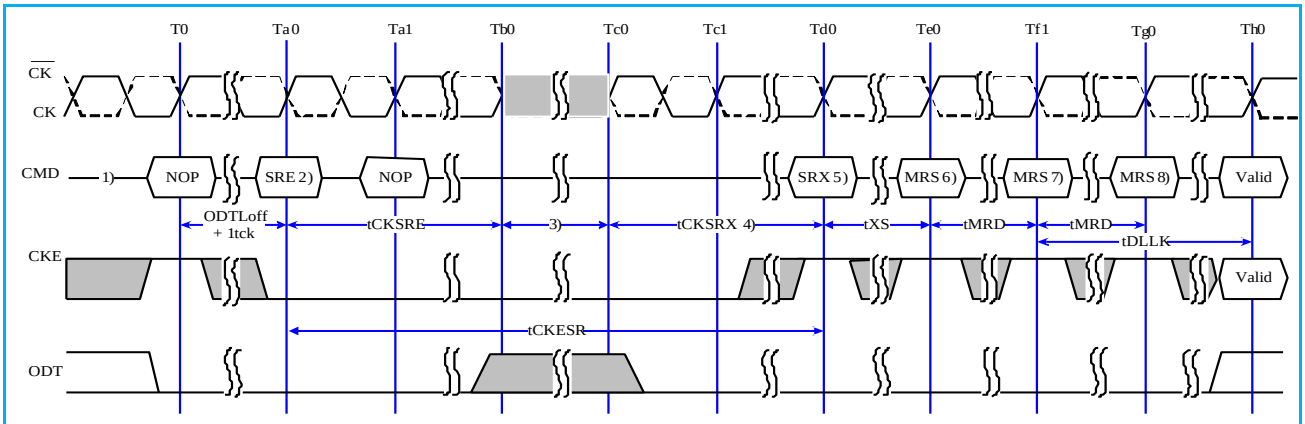


Note:
ODT: Static LOW in case RTT_Nom and RTT_WR is enabled, otherwise static Low or High
1) Starting with Idle State, RTT in Hi-Z State.
2) Disable DLL by setting MR1 Bit A0 to 1.
3) Enter SR.
4) Change Frequency.
5) Clock must be stable at least tCKSRX.
6) Exit SR.
7) Update Mode registers with DLL off parameters setting.
8) Any valid command.

DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with requires frequency change) during Self-Refresh:

1. Starting from Idle state (all banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered).
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with “Input clock frequency change” section.
4. Wait until a stable is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered. the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 Bit A0 to “0” to enable the DLL.
7. Wait tMRD, then set MR0 Bit A8 to “1” to start DLL Reset.
8. Wait tMRD, then set Mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK).
9. Wait for tMOD, then DRAM is ready for next command (remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.



Note:
ODT: Static LOW in case RTT_Nom and RTT_WR is enabled, otherwise static Low or High
1) Starting from Idle State.
2) Enter SR.
3) Change Frequency.
4) Clock must be stable at least tCKSRX.
5) Exit SR.
6) Set DLL-on by MR1 A0="0"
7) Start DLL Reset
8) Any valid command

Input Clock frequency change

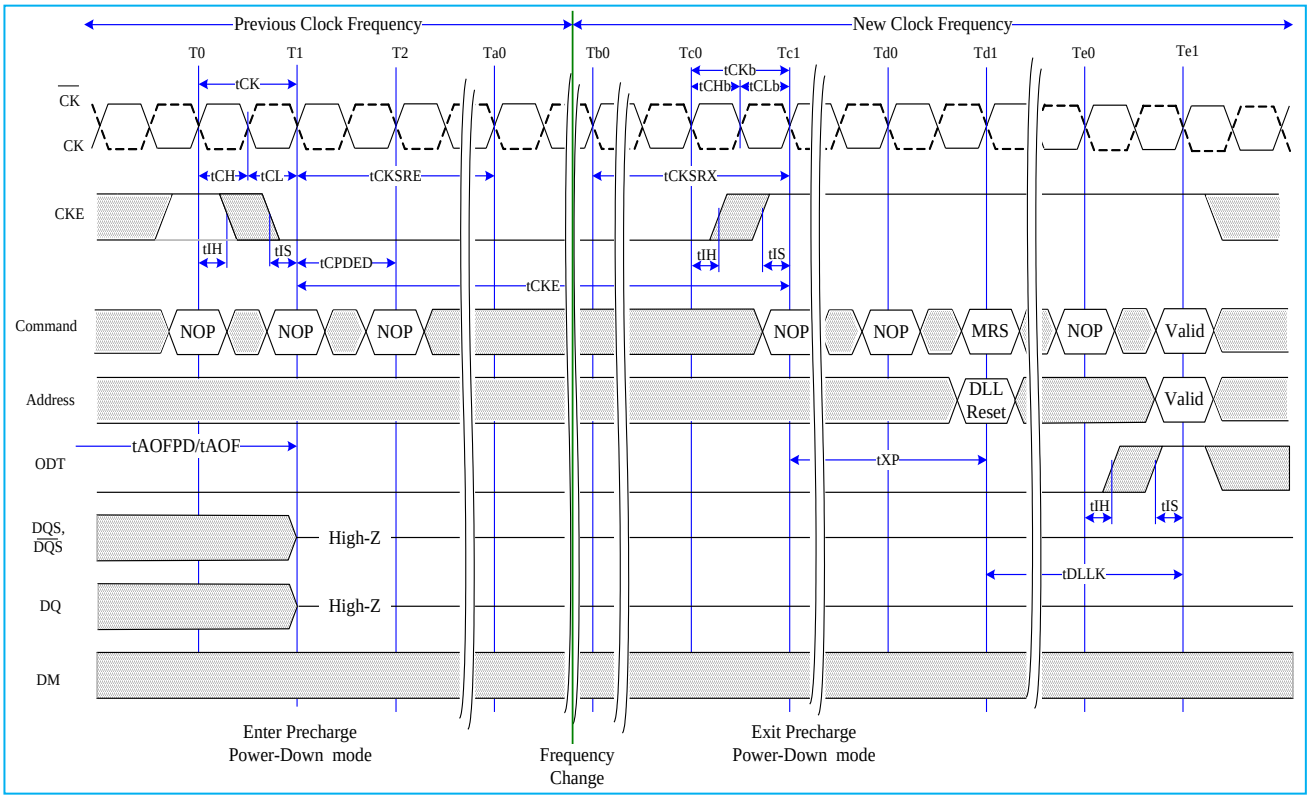
Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specification.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-Down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode of the sole purpose of changing the clock frequency. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade.

The second condition is when the DDR3 SDRAM is in Precharge Power-Down mode (either fast exit mode or slow exit mode). If the RTT_Nom feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_Nom feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before precharge Power Down may be exited; after Precharge Power Down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

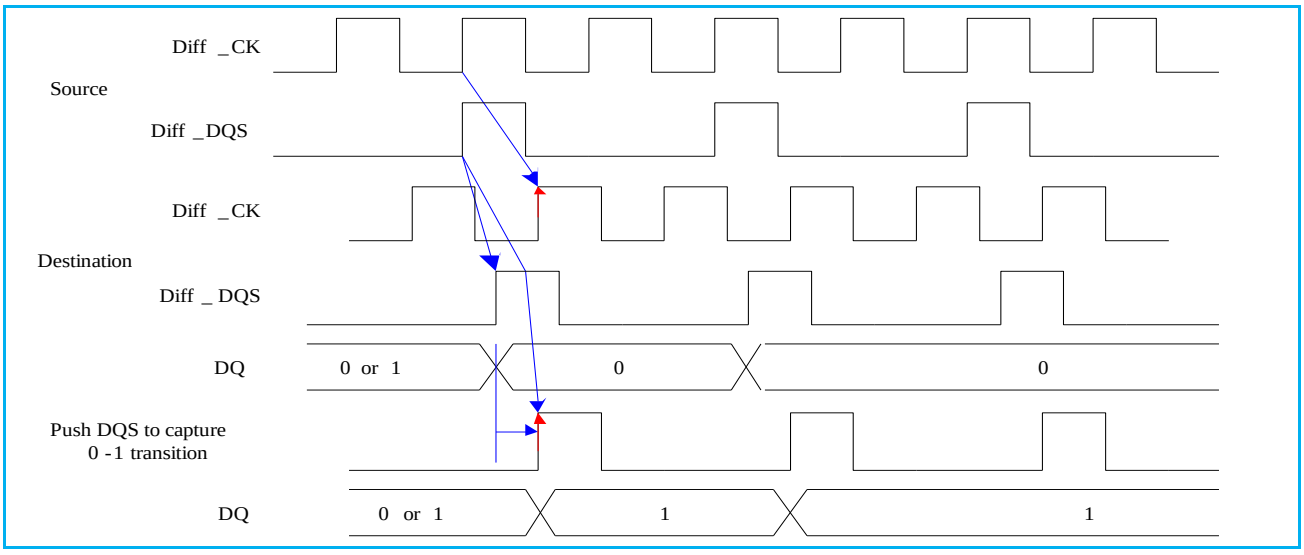
Change Frequency during Precharge Power-down



Write Leveling

For better signal integrity, DDR3 memory adopted fly by topology for the commands, addresses, control signals, and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support “write leveling” in DDR3 SDRAM to compensate the skew.

The memory controller can use the “write leveling” feature and feedback from the DDR3 SDRAM to adjust the DQS - $\overline{\text{DQS}}$ to CK - $\overline{\text{CK}}$ relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - $\overline{\text{DQS}}$ to align the rising edge of DQS - $\overline{\text{DQS}}$ with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK - $\overline{\text{CK}}$, sampled with the rising edge of DQS - $\overline{\text{DQS}}$, through the DQ bus. The controller repeatedly delays DQS - $\overline{\text{DQS}}$ until a transition from 0 to 1 is detected. The DQS - $\overline{\text{DQS}}$ delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS, and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS- $\overline{\text{DQS}}$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in “AC Timing Parameters” section in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is show as below figure.



DQS/$\overline{\text{DQS}}$ driven by the controller during leveling mode must be determined by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations x4, and x8. Therefore, a separate feedback mechanism should be able for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS (diff_LDQS) to clock relationship.

DRAM setting for write leveling and DRAM termination unction in that mode

DRAM enters into Write leveling mode if A7 in MR1 set “High” and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set “Low”. Note that in write leveling mode, only DQS/$\overline{DQS}$ terminations are activated and deactivated via ODT pin not like normal operation.

MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

DRAM termination function in the leveling mode

ODT pin at DRAM	DQS/DQS termination	DQs termination
De-asserted	off	off
Asserted	on	off

Note: In write leveling mode with its output buffer disabled (MR1[bit7]=1 with MR1[bit12]=1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7]=1 with MR1[bit12]=0) only RTT_Nom settings of RZQ/2, RZQ/4, and RZQ/6 are allowed.

Procedure Description

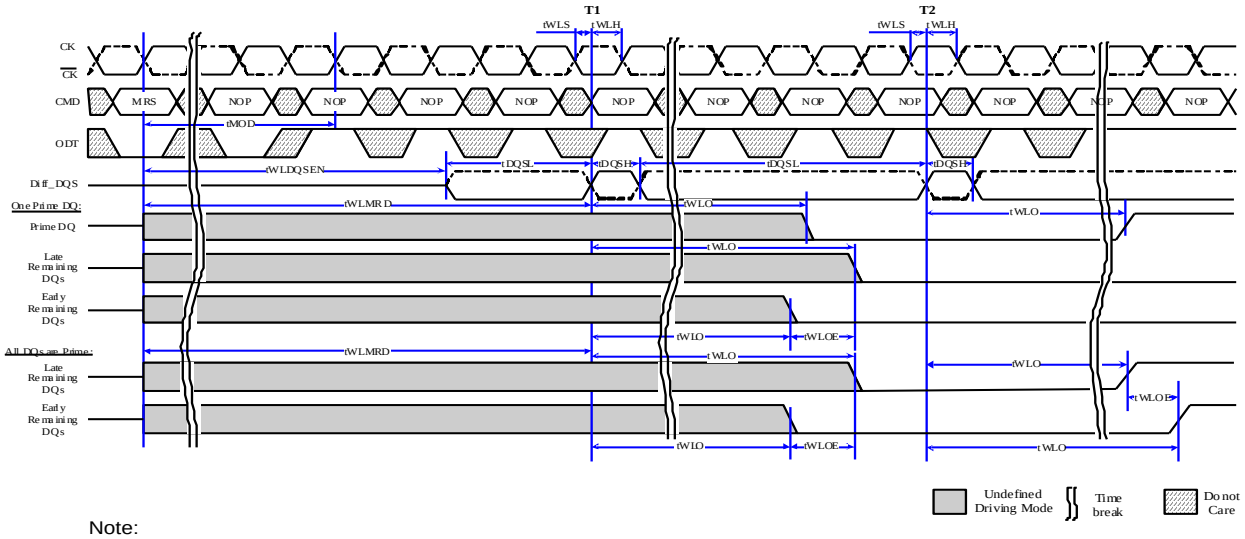
Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or Deselect commands are allowed. As well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other rank must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.

Controller may drive DQS low and $\overline{DQS}$ high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD controller provides a single DQS, $\overline{DQS}$ edge which is used by the DRAM to sample CK – $\overline{CK}$ driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - $\overline{CK}$ status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS/DQS) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS – $\overline{DQS}$ delay setting and launches the next DQS/$\overline{DQS}$ pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS – $\overline{DQS}$ delay setting and write leveling is achieved for the device. The following figure describes the timing diagram and parameters for the overall Write leveling procedure.

Timing details of Write leveling sequence

DQS - $\overline{DQS}$ is capturing CK - $\overline{CK}$ low at T1 and CK - $\overline{CK}$ high at T2



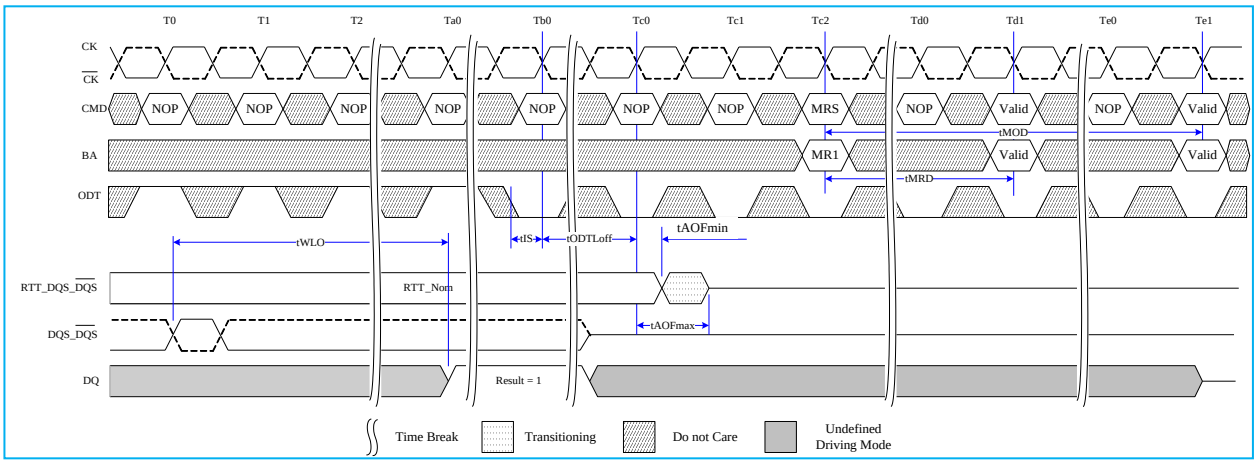
Note:
1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode
3. NOP: NOP or deselect
4. diff_DQS is the differential data strobe (DQS, $\overline{DQS}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{DQS}$ is shown with dotted line.
6. DQS/$\overline{DQS}$ needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

Write Leveling Mode Exit

The following sequence describes how Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and keep it low (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command may be registered. (MR commands may be issued after tMRD (Td1).

Timing detail of Write Leveling exit



Self-Refresh mode summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh mode
0	0	Self-Refresh rate appropriate for the Normal Temperature Range	Normal (0 ~ 85C)
0	1	Self-Refresh appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0 ~ 95C)
1	0	ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-Refresh power consumption is temperature dependent.	Normal (0 ~ 85C)
1	0	ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-Refresh power consumption is temperature dependent.	Normal and Extended (0 ~ 95C)
1	1	Illegal	

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
0	don't care (0 or 1)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Writes will go to DRAM array.
1	See the following table	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

MPR Functional Description

One bit wide logical interface via all DQ pins during READ operation.

Register Read on x4:

DQ [0] drives information from MPR.

DQ [3:1] either drive the same information as DQ [0], or they drive 0.

Register Read on x8:

DQ [0] drives information from MPR.

DQ [7:1] either drive the same information as DQ [0], or they drive 0.

Addressing during for Multi Purpose Register reads for all MPR agents:

BA [2:0]: don't care.

A [1:0]: A [1:0] must be equal to "00". Data read burst order in nibble is fixed.

A[2]: For BL=8, A[2] must be equal to 0, burst order is fixed to [0,1,2,3,4,5,6,7]; For Burst chop 4 cases, the burst order is switched on nibble base, A[2]=0, burst order: 0,1,2,3, A[2]=1, burst order: 4,5,6,7. *)

A [9:3]: don't care.

A10/AP: don't care.

A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0

A11, A13: don't care.

Regular interface functionality during register reads:

Support two Burst Ordering which are switched with A2 and A[1:0]=00.

Support of read burst chop (MRS and on-the-fly via A12/BC).

All other address bits (remaining column addresses bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.

Regular read latencies and AC timings apply.

DLL must be locked prior to MPR READs.

Note *): Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

MPR Register Address Definition

The following table provide an overview of the available data location, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1	00	Read Predefined Pattern for System Calibration	BL8	000	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1	01	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7
			BC4	000	Burst order 0,1,2,3
			BC4	100	Burst order 4,5,6,7
1	10	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7
			BC4	000	Burst order 0,1,2,3
			BC4	100	Burst order 4,5,6,7
1	11	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7
			BC4	000	Burst order 0,1,2,3
			BC4	100	Burst order 4,5,6,7

Note: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for subsequent access. The value on the BA0-BA2 inputs selects the bank, and the addresses provided on inputs A0-A13 selects the row. These rows remain active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle bank) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

READ Operation

Read Burst Operation

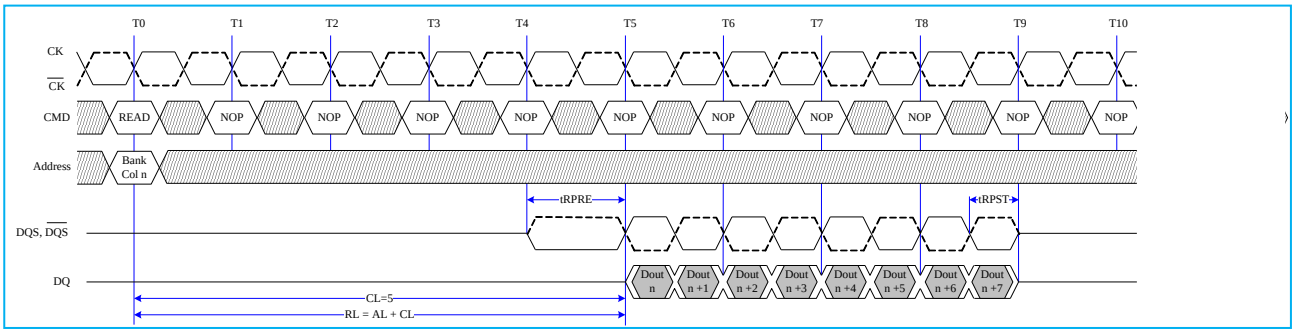
During a READ or WRITE command DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12=0, BC4 (BC4 = burst chop, tCCD=4)

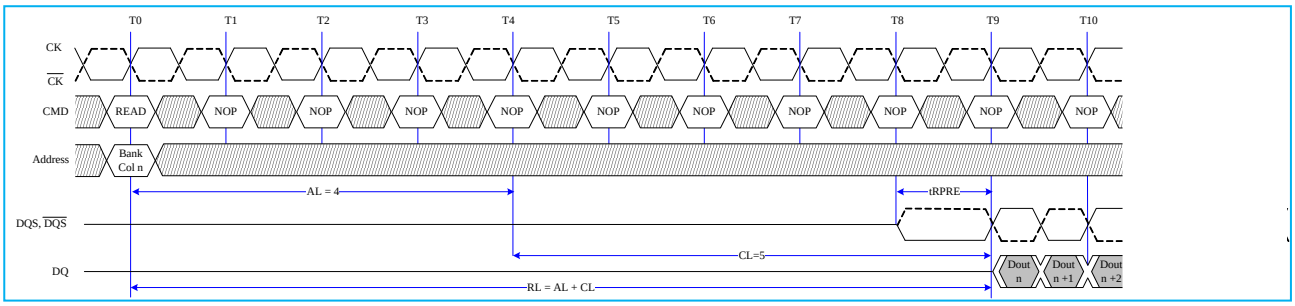
A12=1, BL8

A12 will be used only for burst length control, not a column address.

Read Burst Operation RL=5 (AL=0, CL=5, BL=8)



READ Burst Operation RL = 9 (AL=4, CL=5, BL=8)



READ Timing Definitions

Read timing is shown in the following figure and is applied when the DLL is enabled and locked.

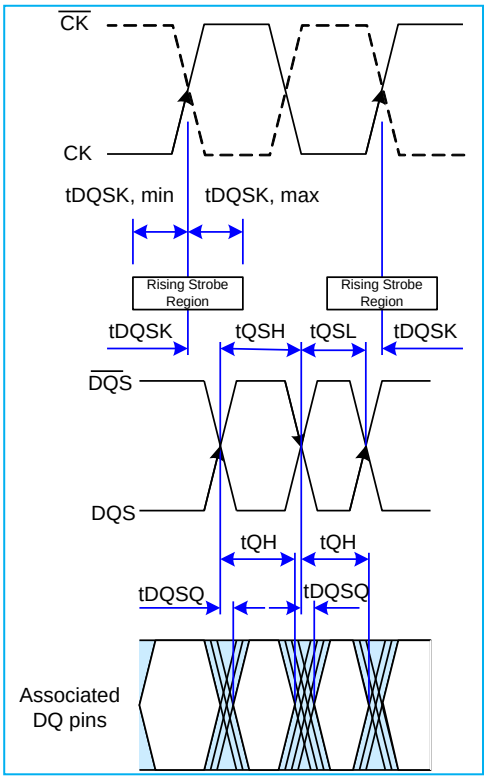
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK.
- tQSH describes the DQS, $\overline{DQS}$ differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS, $\overline{DQS}$ differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Read Timing Definition



Read Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in the following figure and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK and $\overline{CK}$.

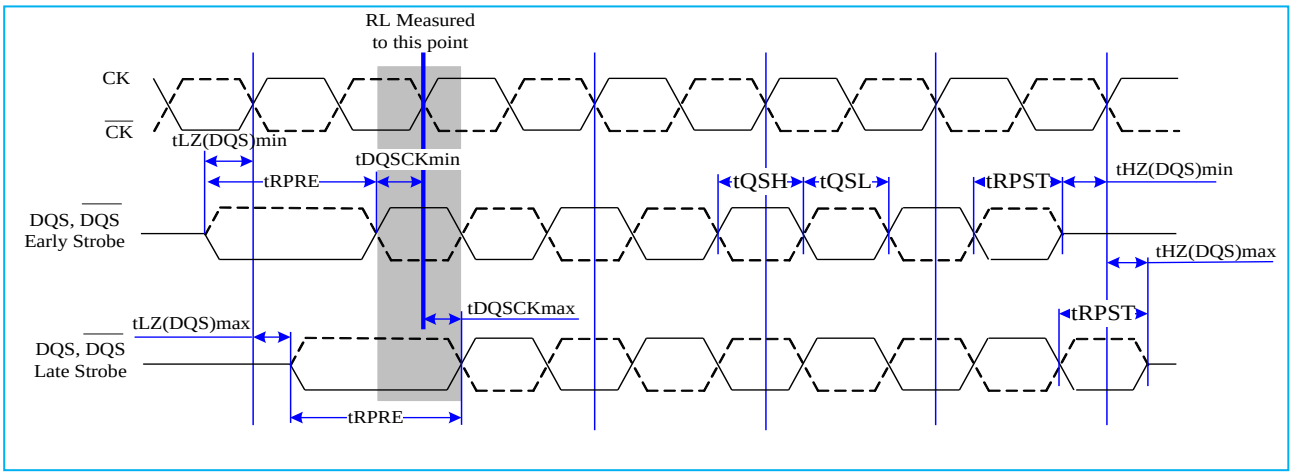
tDQSCK is the actual position of a rising strobe edge relative to CK and $\overline{CK}$.

tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

tDSL describes the data strobe low pulse width

Clock to Data Strobe Relationship



Read Timing; Data Strobe to Data Relationship

The Data Strobe to Data relationship is shown in the following figure and is applied when the DLL and enabled and locked.

Rising data strobe edge parameters:

tDQSQ describes the latest valid transition of the associated DQ pins.

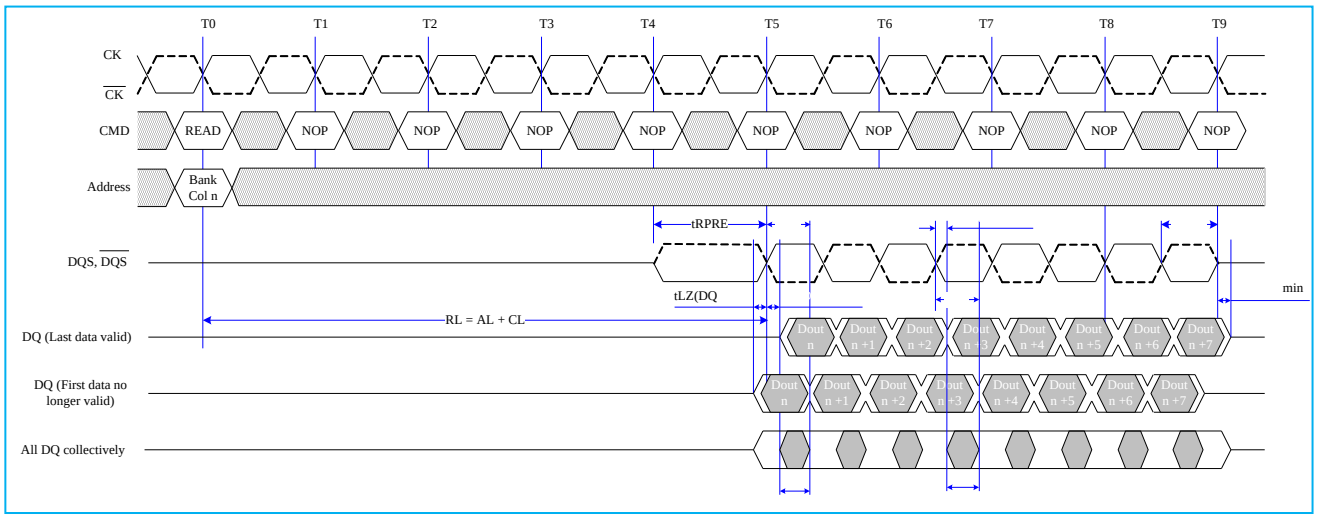
tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

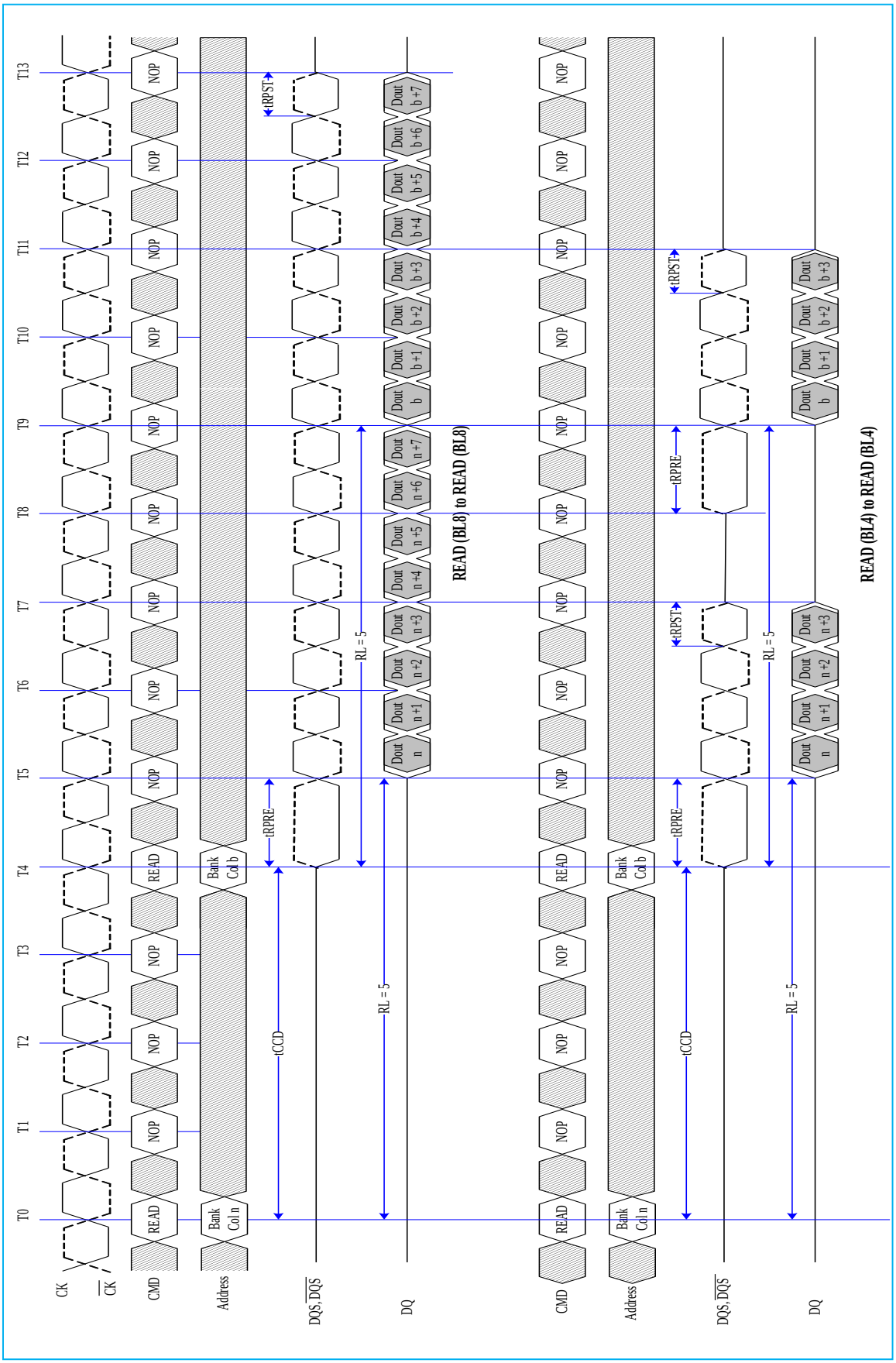
tDQSQ describes the latest valid transition of the associated DQ pins.

tQH describes the earliest invalid transition of the associated DQ pins.

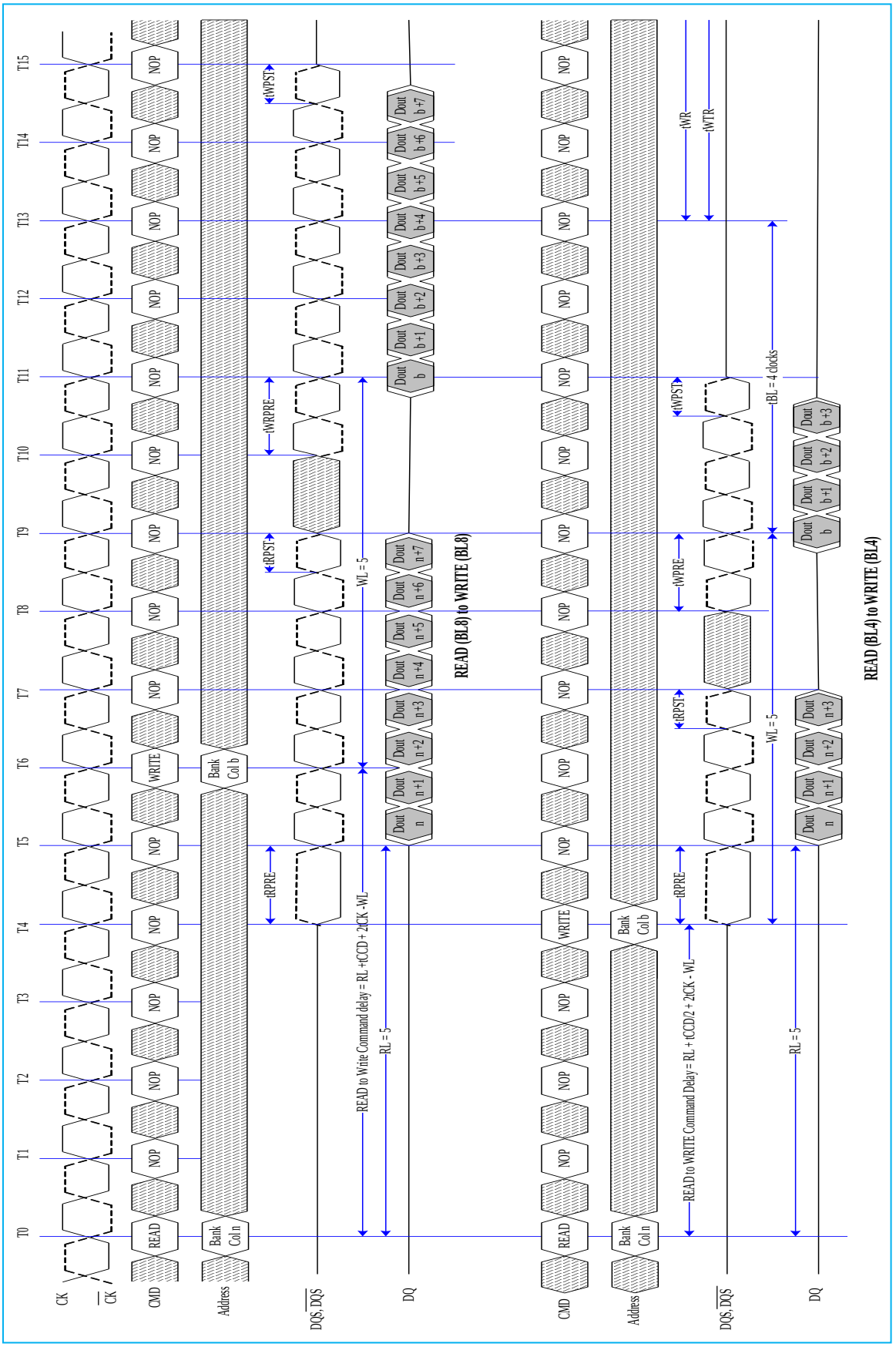
Data Strobe to Data Relationship



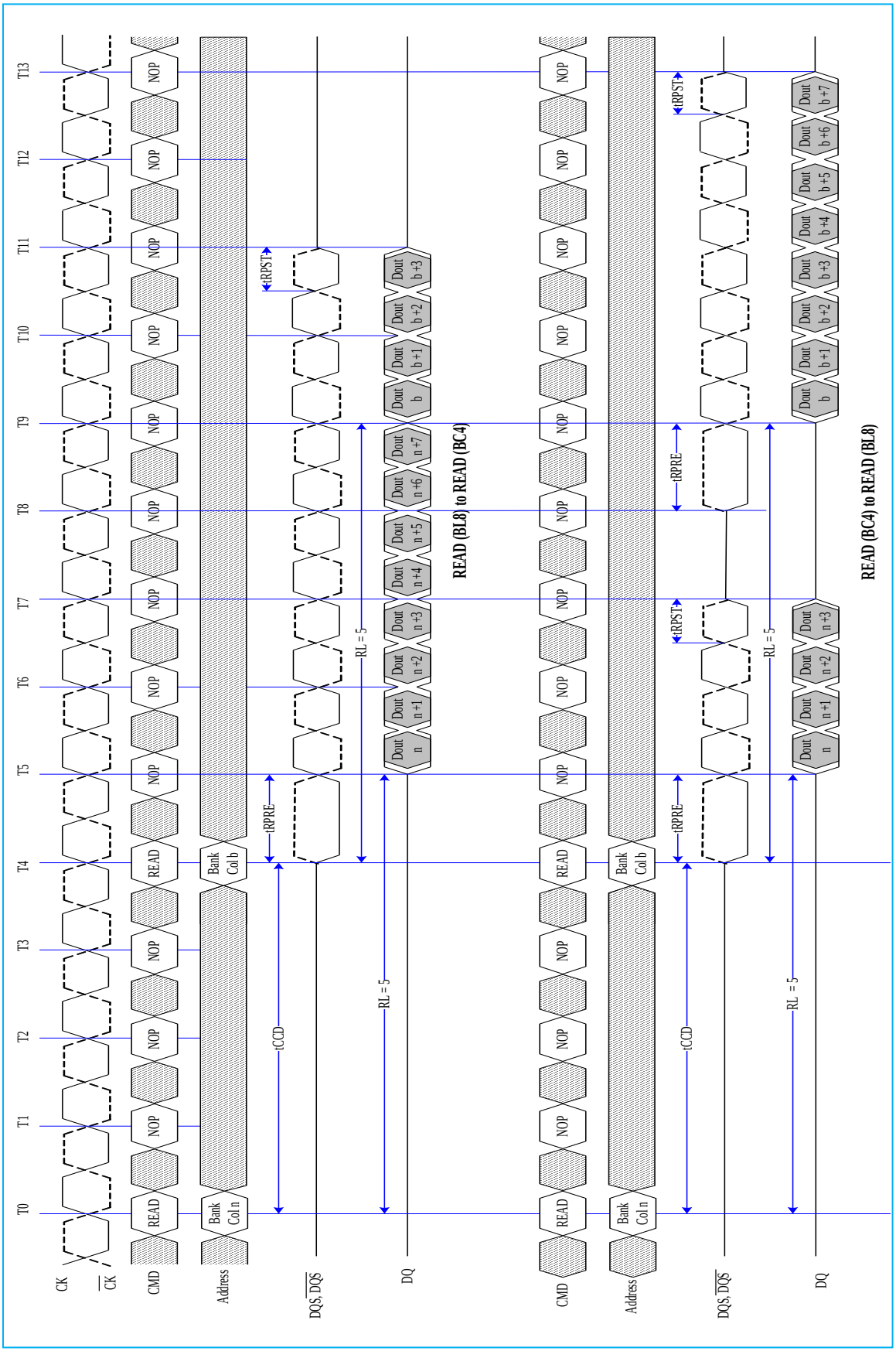
Read to Read (CL=5, AL=0)



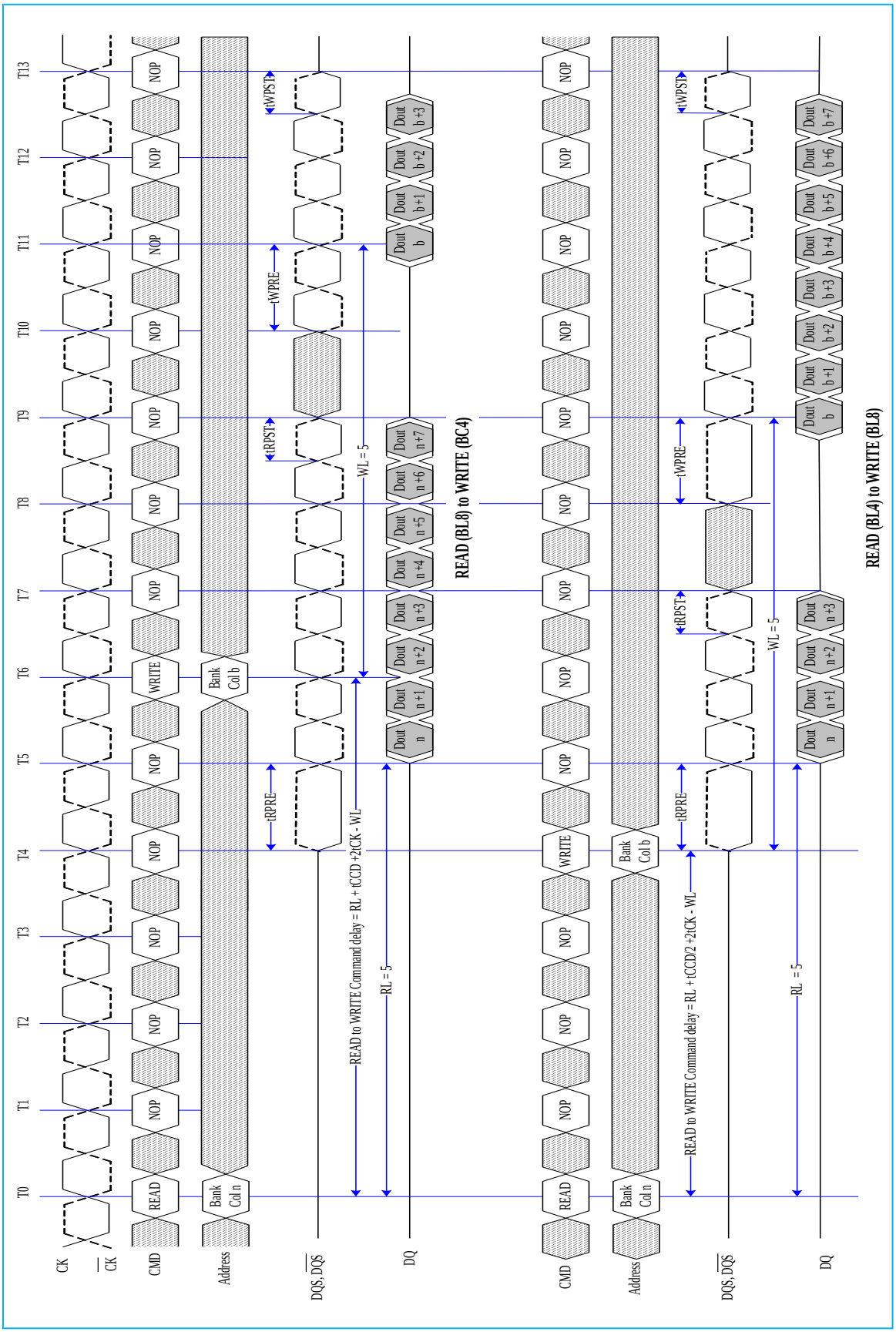
READ to WRITE (CL=5, AL=0; CWL=5, AL=0)



READ to READ (CL=5, AL=0)



READ to WRITE (CL=5, AL=0; CWL=5, AL=0)



Write Operation

DDR3 Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (Auto Precharge can be enabled or disabled).

A12=0, BC4 (BC4 = Burst Chop, tCCD=4)

A12=1, BL8

A12 is used only for burst length control, not as a column address.

WRITE Timing Violations

Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly. However, it is desirable for certain minor violations that the DRAM is guaranteed not to “hang up” and errors be limited to that particular operation.

For the following, it will be assumed that there are no timing violations w.r.t. to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Violations

Should the strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with the offending WRITE command.

Subsequent reads from that location might result in unpredictable read data, however, the DRAM will work properly otherwise.

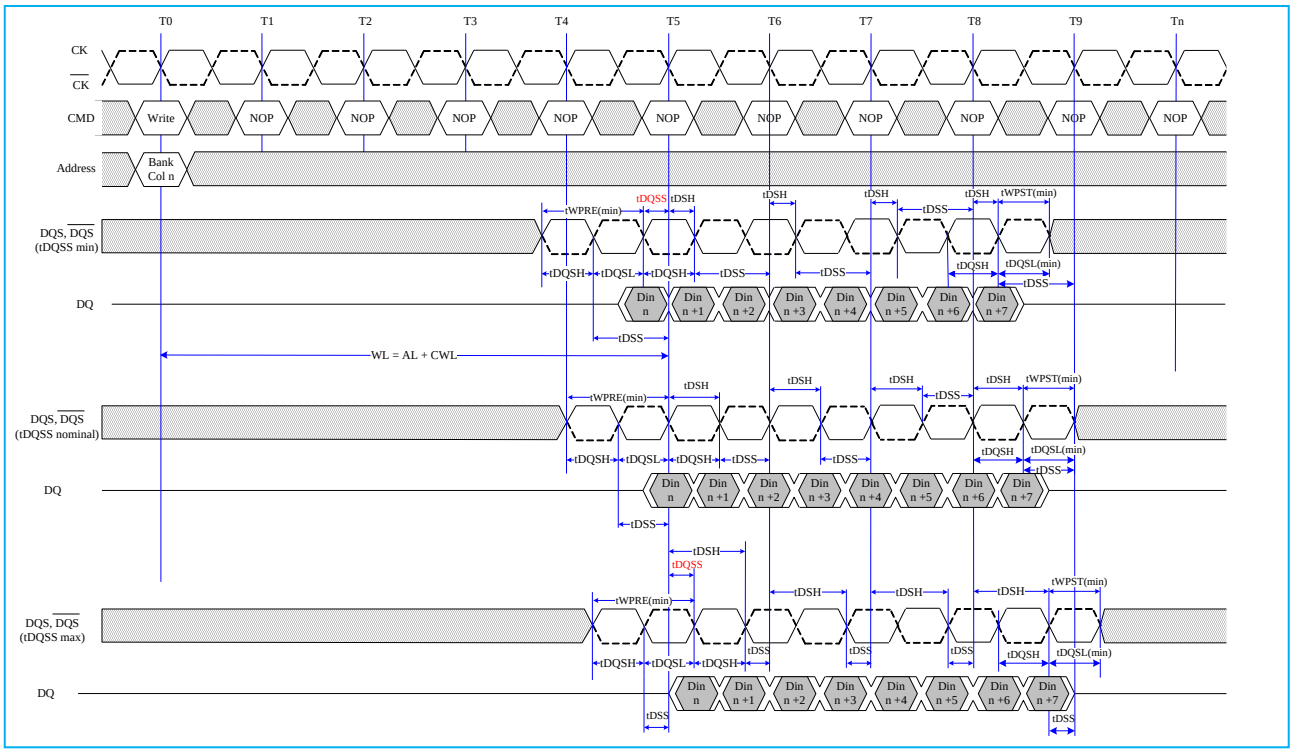
Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that “belong” to a write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).

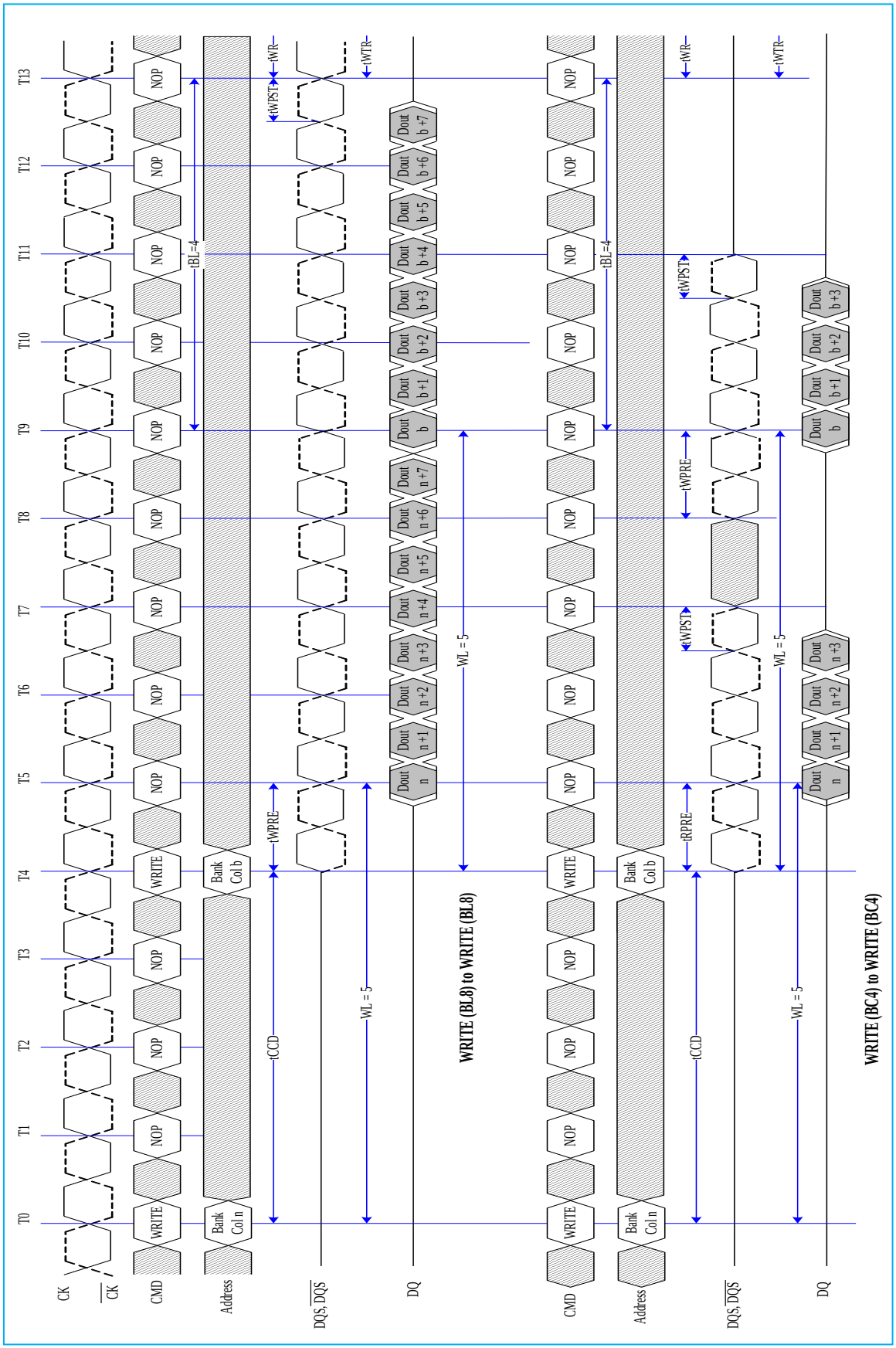
Write Timing Definition



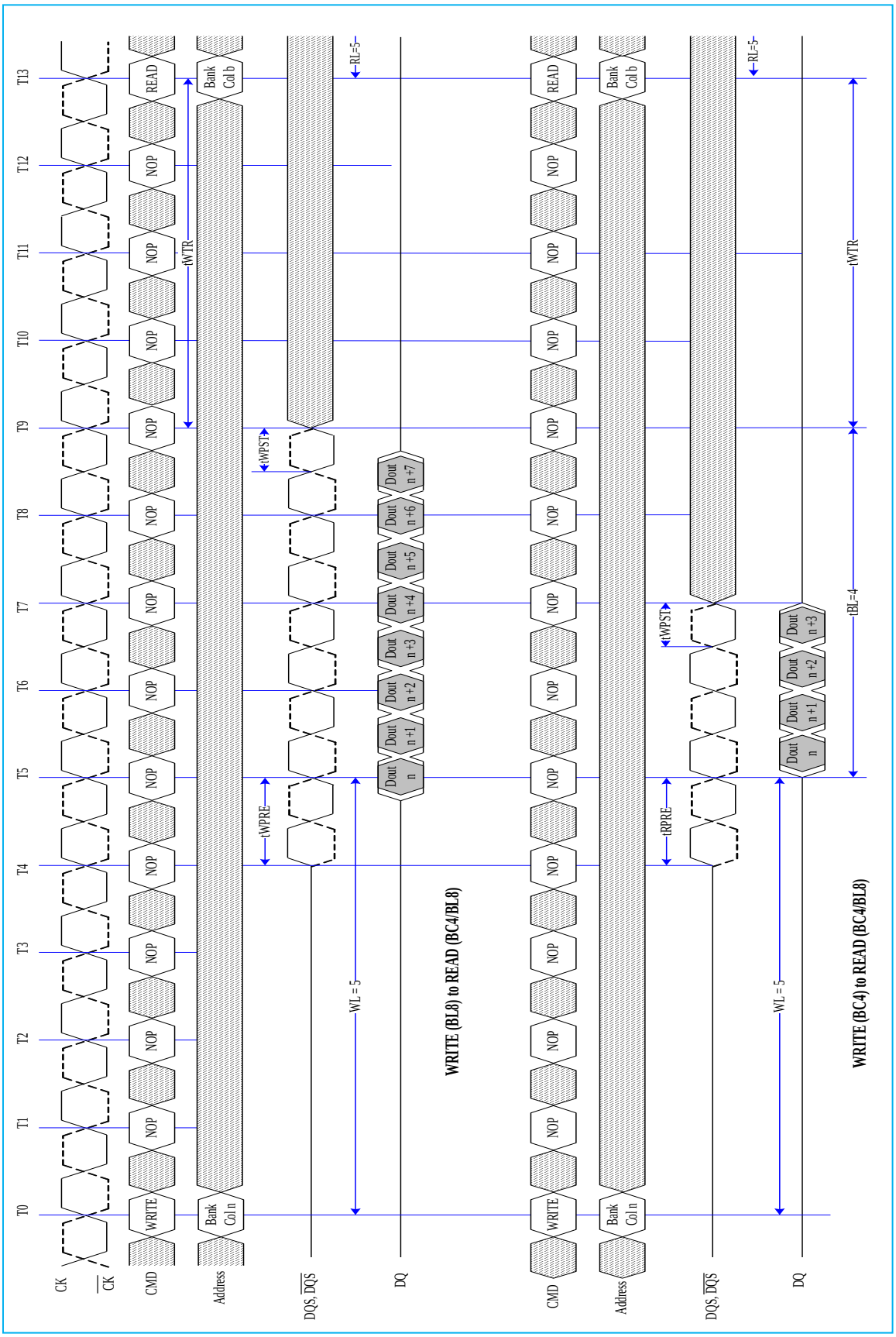
Note:

1. BL=8, WL=5 (AL=0, CWL=5).
2. Din n = data in from column n.
3. NOP commands are shown for ease of illustration; other command may be valid at these times.
4. BL8 setting activated by either MR0 [A1:0=00] or MR0 [A1:0=01] and A12 = 1 during WRITE command at T0.
4. tDQSS must be met at each rising clock edge.

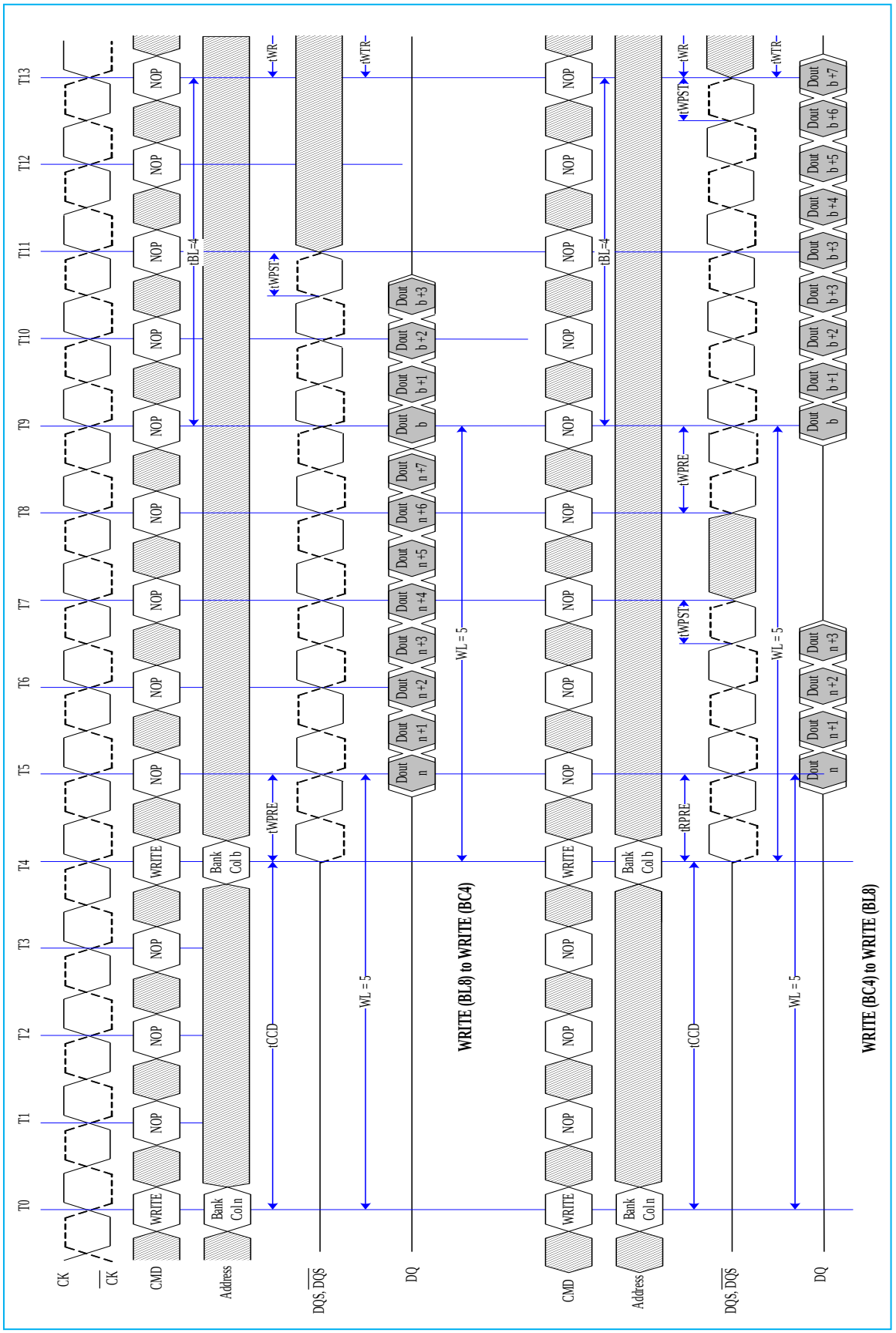
WRITE to WRITE (WL=5; CWL=5, AL=0)



WRITE to READ (RL=5, CL=5, AL=0; WL=5, CWL=5, AL=0; BL=4)



WRITE to WRITE (WL=5, CWL=5, AL=0)

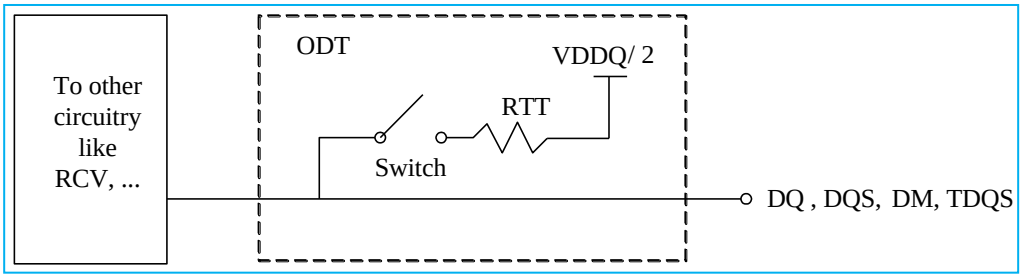


On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{DQS}$, and DM for x4 and x8 configuration and TDQS, $\overline{TDQS}$ for x8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown as below.



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR1 and MR2 are programmed to disable ODT and in self-refresh mode.

ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 {A2, A6, A9} or MR2 {A9, A10} are non-zero. In this case, the value of RTT is determined by the settings of those bits.

Application: Controller sends WR command together with ODT asserted.

One possible application: The rank that is being written to provides termination.

DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR)

DRAM does not use any write or read command decode information.

Termination Truth Table

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 {A2, A6, A9} and MR2{A9, A10} in general)

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

Any bank active with CKE high

Refresh with CKE high

Idle mode with CKE high

Active power down mode (regardless of MR0 bit A12)

Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLonn = WL - 2; ODTLoff = WL-2.

ODT Latency and Posted ODT

In synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For details, refer to DDR3 SDRAM latency definitions.

ODT Latency

Symbol	Parameter	DDR3 SDRAM	Unit
ODTLon	ODT turn on Latency	WL - 2 = CWL + AL - 2	tCK
ODTLoff	ODT turn off Latency	WL - 2 = CWL + AL - 2	tCK

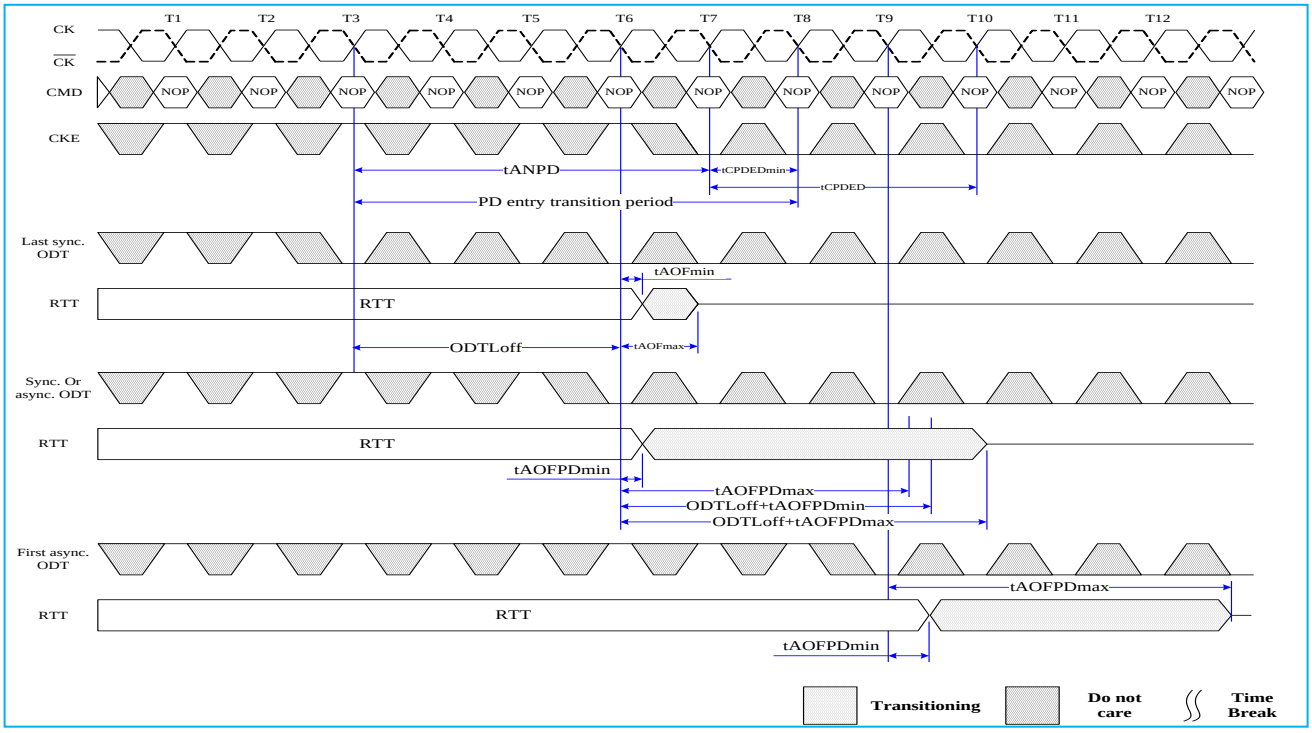
Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

The transition period is defined by the parameters tANPD and tCPDED(min). tANPD is equal to (WL-1) and is counted backwards in time from the clock cycle where CKE is first registered low. tCPDED(min) starts with the clock cycle where CKE is first registered low. The transition period begins with the starting point of tANPD and terminates at the end point of tCPDED(min). If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of tRFC(min) after the Refresh command and the end point of tCPDED(min). Please note that the actual starting point at tANPD is excluded from the transition period, and the actual end point at tCPDED(min) and tRFC(min, respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT changes as early as the smaller of tAONPDmin and (ODTLon*tck+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODTLoff*tCK+tAOFmax). Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL=0; CWL=5; tANPD=WL-1=4)



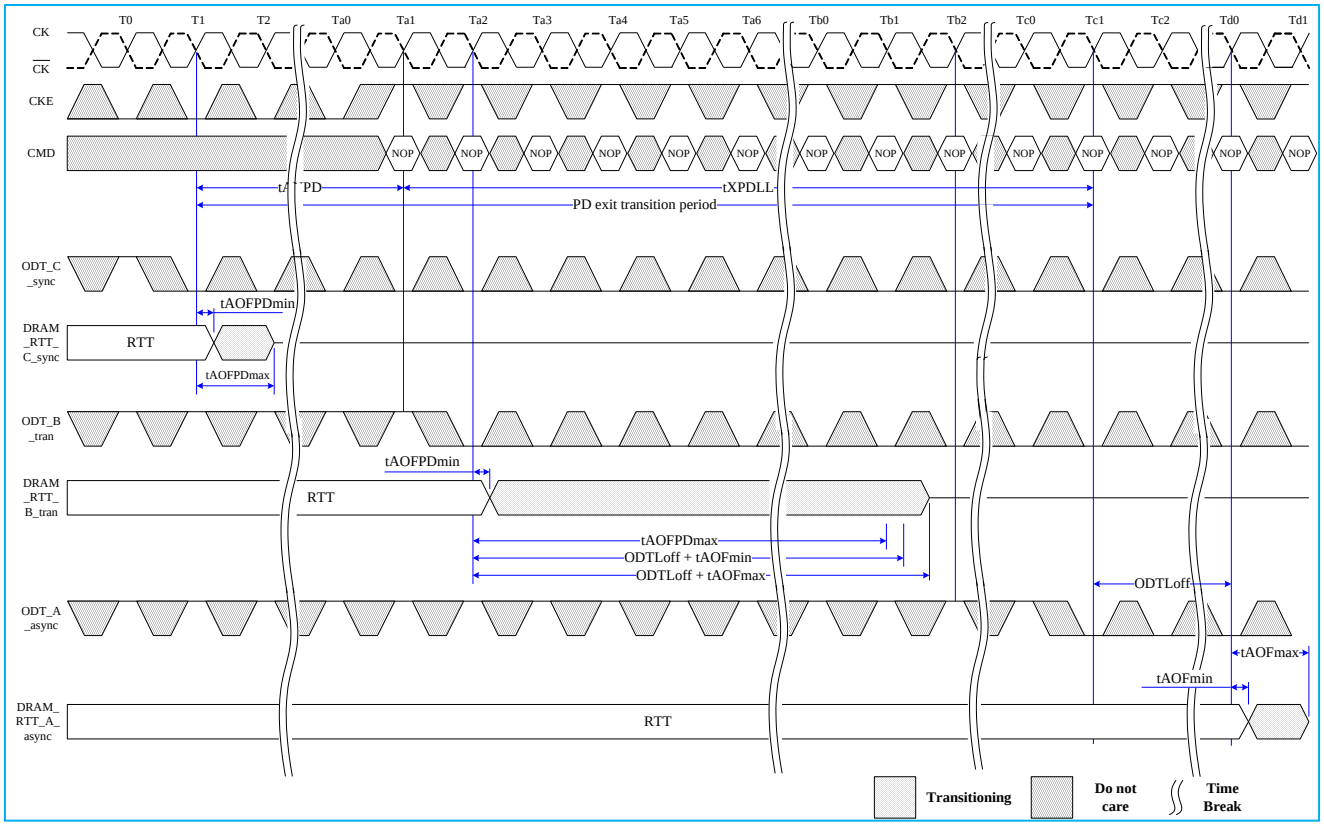
Asynchronous to Synchronous ODT Mode transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

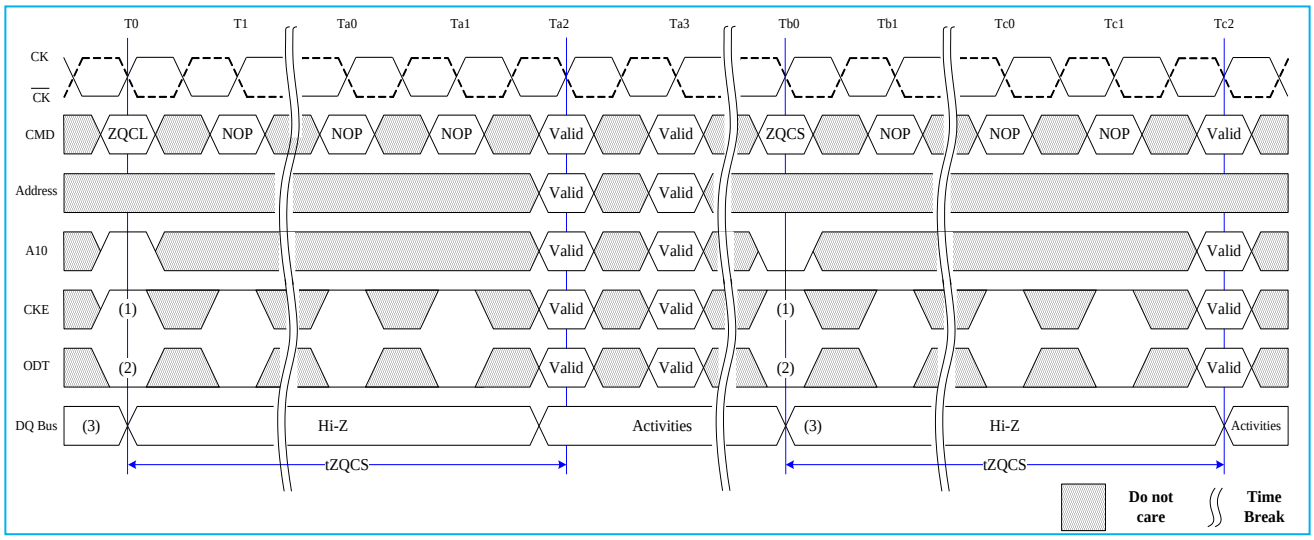
This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL -1) and is counted (backwards) from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of tAONPDmin and (ODT-Lon*tCK+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODToff*tCK+tAOFmax). Note that if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_C, asynchronous response before tANPD; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL=6; AL=CL-1; CWL=5; tANPD=WL-1=9)



ZQ Calibration Timing



Note:

1. CKE must be continuously registered high during the calibration procedure.

2. On-die termination must be disabled via the ODT signal or MRS during the calibration procedure.

3. All devices connected to the DQ bus should be high impedance during the calibration procedure.

ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pin relative to Vss	-0.4 ~ 1.975	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.975	V	1,3
Vin, Vout	Voltage on any pin relative to Vss	-0.4 ~ 1.975	V	1
Tstg	Storage Temperature	-55 ~ 100	°C	1,2

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6VDDQ, when VDD and VDDQ are less than 500mV; Vref may be equal to or less than 300mV.

Temperature Range

Symbol	Parameter	Rating	Units	Notes
Toper	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3

Note:

1. Operating Temperature Toper is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional apply:

a) Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1x refresh (tREFI to 7.8us) in the Extended Temperature Range.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2
VDD	Supply Voltage	1.28	1.35	1.45	V	1,2
VDDQ	Supply Voltage for Output	1.28	1.35	1.45	V	1,2

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

AC & DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals & Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		Unit	Note
		Min.	Max.		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	V	1
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	V	1
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note2	V	1,2
VIL.CA(AC175)	AC input logic low	Note2	Vref - 0.175	V	1,2
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note2	V	1,2
VIL.CA(AC150)	AC input logic low	Note2	Vref - 0.150	V	1,2
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3,4

Note:

1. For input only pins except RESET.Vref=VrefCA(DC)
2. See "Overshoot and Undershoot Specifications"
3. The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 0.1% VDD.
4. For reference: approx. VDD/2 +/- 15mV.
5. To allow VREFCA margining, all DRAM Command and Address Input Buffers MUST use external VREF (provided by system) as the input for their VREFCA pins. All VIH/L input level MUST be compared with the external VREF level at the 1st stage of the Command and Address input buffer

AC and DC Logic Input Levels for Single-Ended Signals & DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		Unit	Note
		Min.	Max.	Min.	Max.		
VIH.DQ(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.DQ(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.DQ(AC175)	AC input logic high	Vref + 0.175	Note2	Vref + 0.150	Note2	V	1,2,5
VIL.DQ(AC175)	AC input logic low	Note2	Vref - 0.175	Note2	Vref - 0.150	V	1,2,5
VIH.DQ(AC150)	AC input logic high	Vref + 0.150	Note2	Vref + 0.150	Note2	V	1,2,5
VIL.DQ(AC150)	AC input logic low	Note2	Vref - 0.150	Note2	Vref - 0.150	V	1,2,5
VREFDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3,4
VREFDQ_t(DC)	Reference Voltage for trained DQ, DM inputs	**0.45 * VDD**	**0.55 * VDD**	**0.45 * VDD**	**0.55 * VDD**	**V**	**3,4 6,7**

Note:

1. For input only pins except $\overline{\text{RESET}}$. Vref = VrefDQ(DC)
2. See "Overshoot and Undershoot Specifications"
3. The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than ± 0.1% VDD.
4. For reference: approx. VDD/2 ±15mV.
5. Single-ended swing requirement for DQS-$\overline{\text{DQS}}$, is 350mV (peak to peak). Differential swing requirement for DQS-$\overline{\text{DQS}}$, is 700mV (peak to peak)
6. VRefDQ training is performed only during system boot. Once the training is completed and an optimal VRefDQ_t(DC) voltage level is identified, the optimal VRefDQ_t(DC) voltage level will be used during system runtime. During VRefDQ training, VRefDQ is swept from 40% of VDD to 60% of VDD to find the optimal VRefDQ_t(DC) voltage level; and once the optimal VRefDQ_t(DC) is set, it must stay within +/- 1% of its set value as well as not be less than 45% of VDD or exceed 55% of VDD. VIH.DQ(AC)min/VIL.DQ(AC)max = Optimal VRefDQ_t(DC) +/- AC Level, where "AC Level" is the actual AC voltage level per DDR3 speed bins as specified in JESD79-3 specification. After VRefDQ training is completed and the optimal VRefDQ_t(DC) is set, the Memory Controller provides the DRAM device a valid write window. Through DQS placement optimization and VRefDQ centering, the valid write window is optimized for both input voltage margin and tDS+tDH window for the DRAM receiver. The DRAM device supports the use of the above techniques to optimize the write timing and voltage margin, as long as the technique does not create any DIMM failures due to DRAM input voltage and/or timing spec violations as defined in JESD79-3 specification.
7. To allow VREFDQ margining, all DRAM Data Input Buffers MUST use external VREF (provided by system) as the input for their VREFDQ pins. All VIH/L input level MUST be compared with the external VREF level at the 1st stage of the Data input buffer.

Vref Tolerances

The dc-tolerance limits and ac-moist limits for the reference voltages V_{refCA} and V_{refDQ} are illustrated in the following figure. It shows a valid reference voltage $V_{ref}(t)$ as a function of time. (V_{ref} stands for V_{refCA} and V_{refDQ} likewise).

$V_{ref}(DC)$ is the linear average of $V_{ref}(t)$ over a very long period of time (e.g.,1 sec). This average has to meet the min/max requirement in previous page. Furthermore $V_{ref}(t)$ may temporarily deviate from $V_{ref}(DC)$ by no more than ±1% VDD.

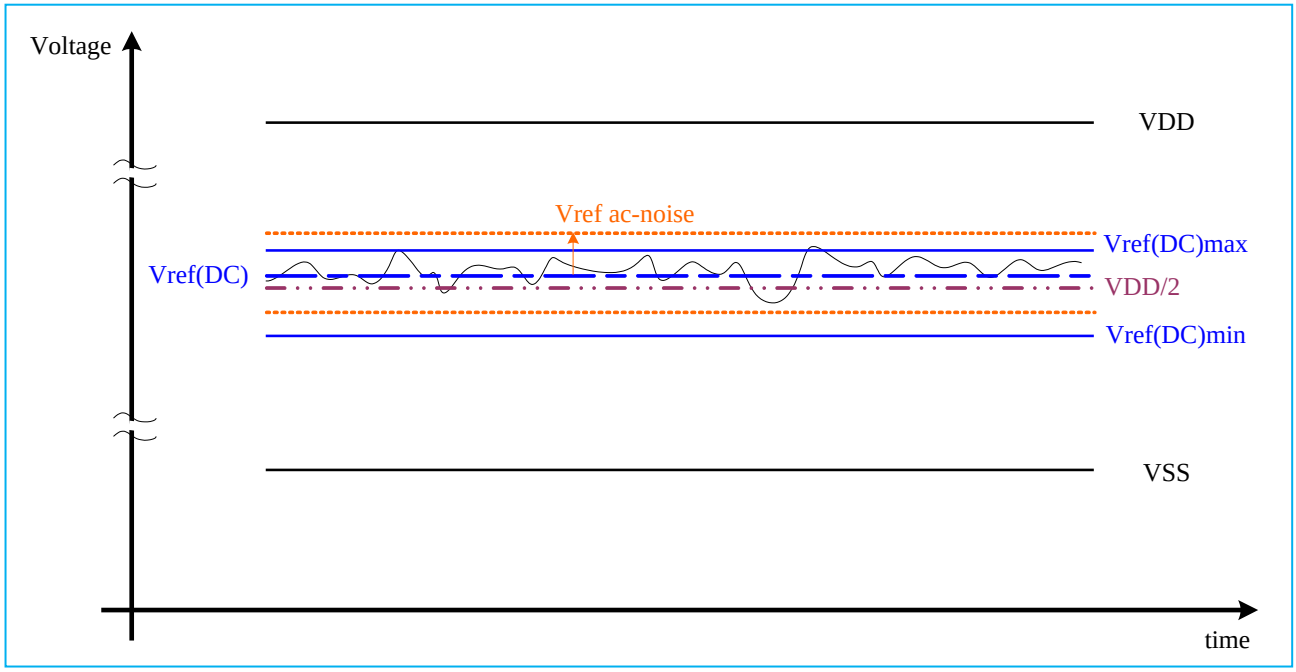
The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC), and VIL(DC) are dependent on V_{ref}.

"V_{ref}" shall be understood as $V_{ref}(DC)$.

The clarifies that dc-variations of V_{ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{ref}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and de-rating values need to include time and voltage associated with V_{ref} ac-noise. Timing and voltage effects due to ac-noise on V_{ref} up to the specified limit (±1% of VDD) are included in DRAM timing and their associated de-ratings.

Illustration of $V_{ref(DC)}$ tolerance and V_{ref}ac-noise limits

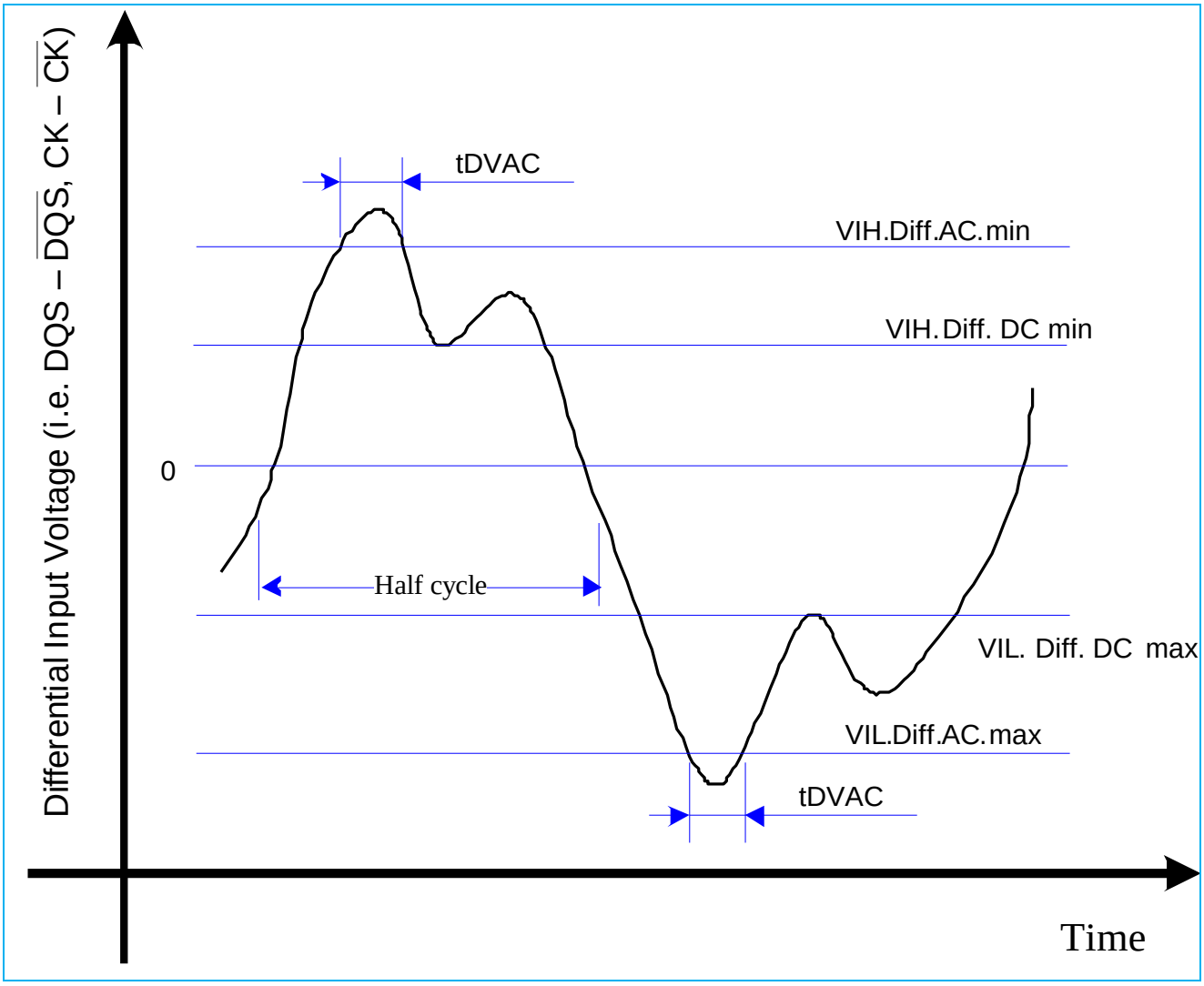


AC and DC Logic Input Levels for Differential Signals

Symbol	Parameter	DDR3-800, 1066, 1333, & 1600		Unit	Notes
		Min.	Max.		
V_{IHdiff}	Differential input logic high	+0.200	Note3	V	1
V_{ILdiff}	Differential input logic low	Note3	-0.200	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (VIH(ac) – Vref)	Note3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	Note3	2 x (Vref - VIL(ac))	V	2

Note:
1. Used to define a differential signal slew-rate.
2. For CK - CK use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS, DQSL, DQSL, DQSU, DQSU use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also there.
3. These values are not defined, however the single-ended signals CK, CK, DQS, DQS, DQSL, DQSL, DQSU, DQSU need to be within the respective limits (VIH(dc)max, VIL(dc)min) for single-ended signals as well as limitations for overshoot and undershoot.

Definition of differential ac-swing and “time above ac-level”



Allowed time before ring-back (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	tDVAC [ps] @IVIH/Ldiff(ac)I = 350mV		tDVAC [ps] @IVIH/Ldiff(ac)I = 300mV	
	min	max	min	max
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, or $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(ac) / VIL(ac)) for ADD/CMD signals) in every half-cycle. DQS, DQSL, DQSU, DQS, DQSL, DQSL have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH(ac) / VIL(ac)) for DQ signals) in every half-cycle proceeding and following a valid transition.

Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, or $\overline{DQSU}$

Symbol	Parameter	DDR3-800, 1066, 1333, & 1600		Unit	Notes
		Min	Max		
VSEH	Single-ended high-level for strobes	(VDDQ/2) + 0.175	note3	V	1, 2
	Single-ended high-level for CK, CK	(VDDQ/2) + 0.175	note3	V	1, 2
VSEL	Single-ended low-level for strobes	note3	(VDDQ/2) - 0.175	V	1, 2
	Single-ended Low-level for CK, CK	note3	(VDDQ/2) - 0.175	V	1, 2

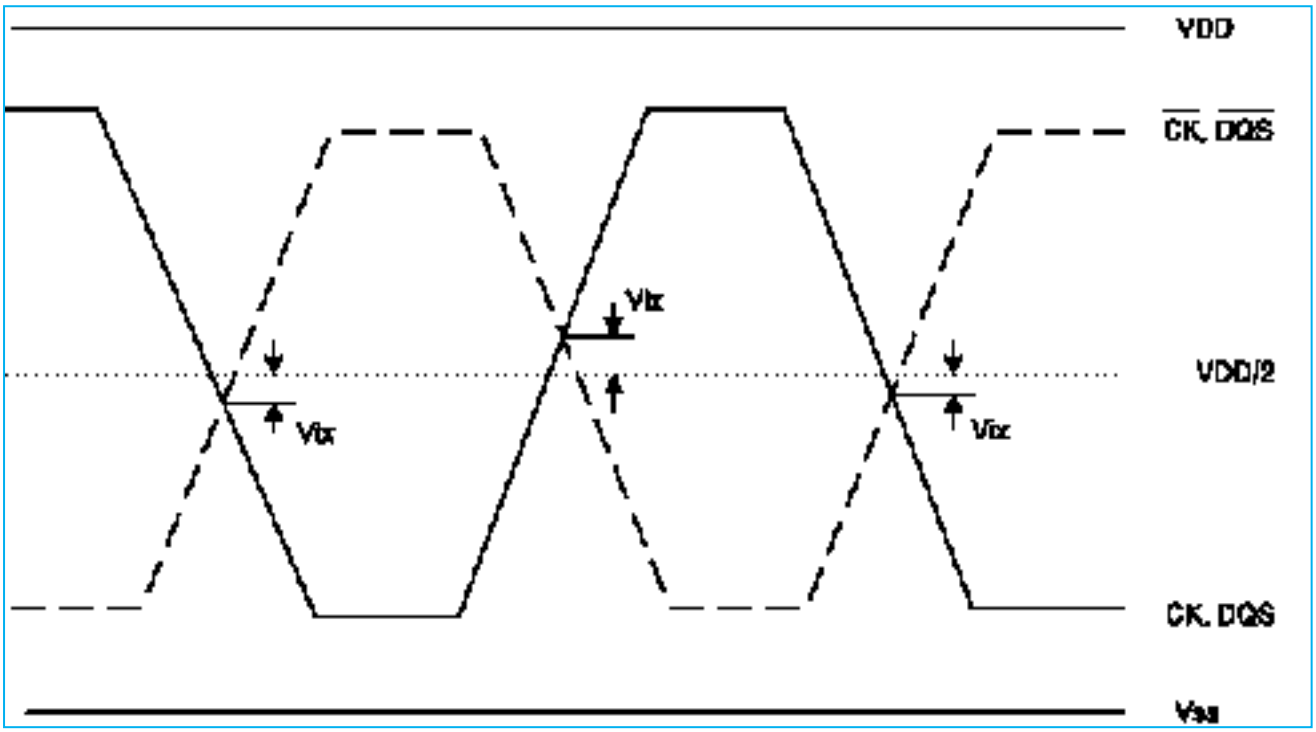
Note:

1. For CK, CK use VIH/VIL(ac) of ADD/CMD; for strobes (DQS, DQSL, DQSU, CK, DQS, DQSL, or DQSU) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also there.
3. These values are not defined, however the single-ended signals CK, CK, DQS, DQS, DQSL, DQSL, DQSU, DQSU need to be within the respective limits (VIH(dc)max, VIL(dc)min) for single-ended signals as well as limitations for overshoot and undershoot.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK and DQS, DQS) must meet the requirements in the following table. The differential input cross point voltage Vix is measured from the actual cross point of true and complete signal to the midlevel between of VDD and VSS.

Vix Definition



Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800, 1066, 1333, & 1600		Unit	Note
		Min.	Max.		
Vix	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK	-150	150	mV	
		-175	175	mV	1
	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS	-150	150	mV	

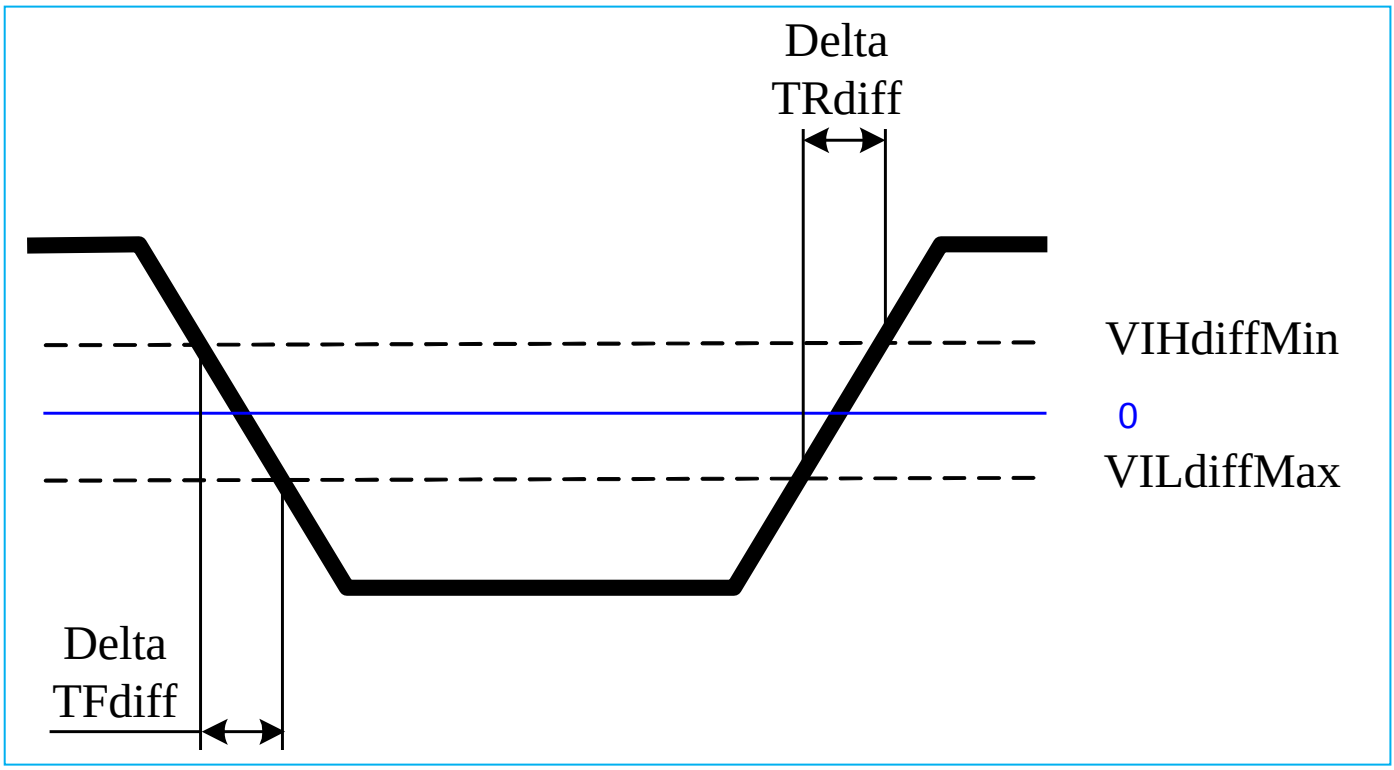
Note1: Extended range for Vix is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 ± 250mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3V/ns.

Slew Rate Definition for Differential Input Signals

Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$ & DQS-$\overline{DQS}$)	VILdiffmax	VIHdiffmin	[VIHdiffmin-VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$ & DQS-$\overline{DQS}$)	VIHdiffmin	VILdiffmax	[VIHdiffmin-VILdiffmax] / DeltaTFdiff
The differential signal (i.e., CK-$\overline{CK}$ & DQS-$\overline{DQS}$) must be linear between these thresholds.			

Input Nominal Slew Rate Definition for single ended signals



AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8xVDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5xVDDQ	V	
VOL(DC)	DC output low measurement level (fro IV curve linearity)	0.2xVDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT+0.1xVDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT-0.1xVDDQ	V	1

Note:

1. The swing of ±0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2.

Differential AC and DC Output Levels

Symbol	Parameter	DDR3	Unit	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

Note:

1. The swing of ± 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT=VDDQ/2 at each of the differential outputs.

Package Dimensions (x8; 78 balls; 0.8mmx0.8mm Pitch; BGA)