Delson
Technology Co, Ltd.

D73CAG01168CF
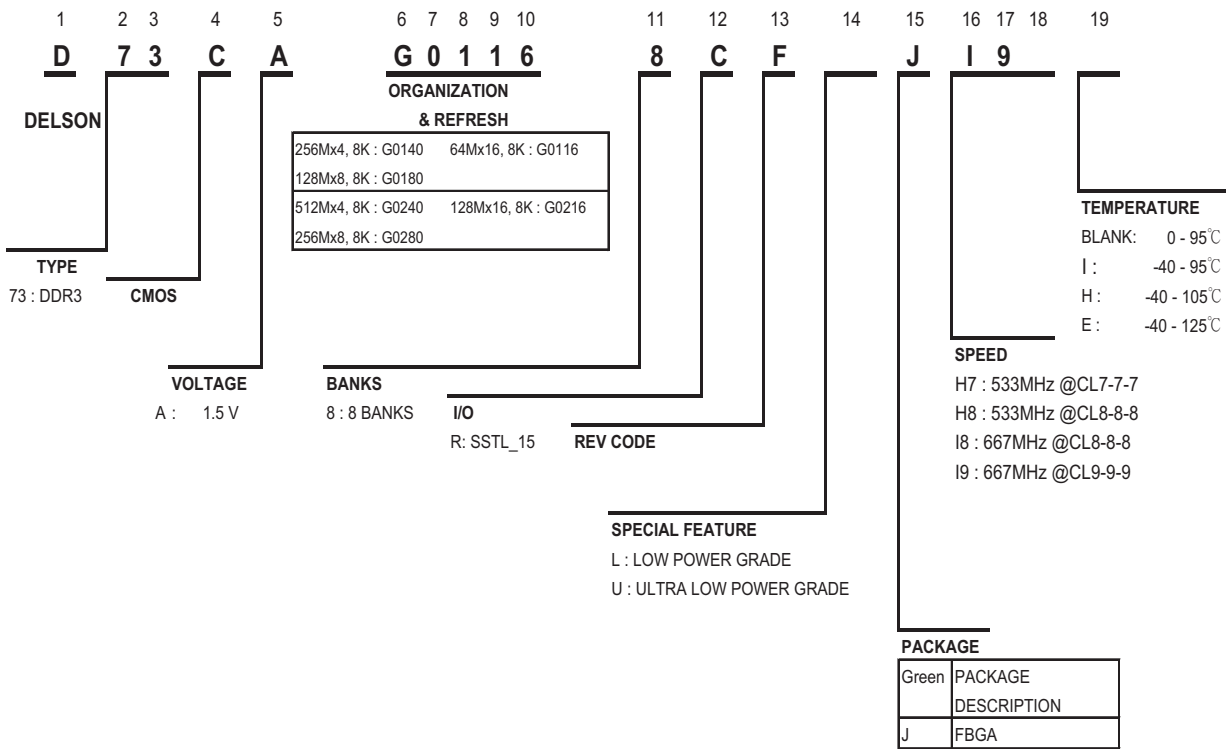## HIGH PERFORMANCE 1Gbit DDR3 SDRAM
8 BANKS X 16Mbit X 8

- 1.35V -0.067/+0.1V &1.5V ± 0.075V (JEDEC Standard Power Supply)
- 8 Internal memory banks (BA0- BA2)
- Differential clock input (CK, $\overline{CK}$)
- Programmable $\overline{CAS}$ Latency: 5, 6, 7, 8, 9, 10, 11, 12, 13, (14)
- POSTED CAS ADDITIVE Programmable Additive Latency: 0, CL-1, CL-2
- Programmable Sequential / Interleave Burst Type
- Programmable Burst Length: 4, 8
- 8n-bit prefetch architecture
- Output Driver Impedance Control
- Differential bidirectional data strobe
- Write Leveling

- OCD Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- Auto Self-Refresh
- Self-Refresh Temperature
- RoHS Compliance
- Lead-Free and Halogen-Free
- Packages:
  78-Ball BGA for x8 components
  96-Ball BGA for x16 components
- Operation Temperture
  Commerical grade ($0°C \leq TC \leq 95°C$)
  - CF

Part Number Information

Part number breakdown diagram with positions 1-19:

D 7 3 C A G 0 1 1 6 8 C F J I 9

Position 1: **D** — **DELSON**

Positions 2,3: **7 3** — **TYPE** — 73 : DDR3

Position 4: **C** — **CMOS**

Position 5: **A** — **VOLTAGE** — A : 1.5 V

Positions 6-10: **G 0 1 1 6** — **ORGANIZATION & REFRESH**

256Mx4, 8K : G0140	64Mx16, 8K : G0116
128Mx8, 8K : G0180	
512Mx4, 8K : G0240	128Mx16, 8K : G0216
256Mx8, 8K : G0280	

Position 11: **8** — **BANKS** — 8 : 8 BANKS

I/O — R: SSTL_15

Position 12: **C** — **REV CODE**

Position 13: **F** — **SPECIAL FEATURE** — L : LOW POWER GRADE / U : ULTRA LOW POWER GRADE

Position 14: — **PACKAGE**

Green	PACKAGE DESCRIPTION
J	FBGA

*GREEN: RoHS-compliant and Halogen-Free

Position 15: **J** — **SPEED**
- H7 : 533MHz @CL7-7-7
- H8 : 533MHz @CL8-8-8
- I8 : 667MHz @CL8-8-8
- I9 : 667MHz @CL9-9-9

Positions 16,17,18: **I 9** — **TEMPERATURE**
- BLANK: 0 - 95℃
- I : -40 - 95℃
- H : -40 - 105℃
- E : -40 - 125℃

Description

The 1Gb Double-Data-Rate-3 (DDR3) DRAMs is double data rate architecture to achieve high-speed operation. It is internally configured as an eight bank DRAM.

The 1Gb chip is organized as 16Mbit x 8 I/Os x 8 banks or 8Mbit x 16 I/Os x 8 bank devices. These synchronous devices achieve high speed double-data-rate transfer rates of up to 2133 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3 DRAM   key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V &1.35V -0.067/+0.1V power supply and are available in BGA packages.

Fig. 1: Pin Configuration – 78 balls BGA Package (x8)

< TOP View>

See the balls through the package

	1	2	3		7	8	9
A	VSS	VDD	NC		NU/$\overline{TDQS}$	VSS	VDD
B	VSS	VSSQ	DQ0		DM/TDQS	VSSQ	VDDQ
C	VDDQ	DQ2	DQS		DQ1	DQ3	VSSQ
D	VSSQ	DQ6	$\overline{DQS}$		VDD	VSS	VSSQ
E	VREFDQ	VDDQ	DQ4		DQ7	DQ5	VDDQ
F	NC	VSS	$\overline{RAS}$		CK	VSS	NC
G	ODT	VDD	$\overline{CAS}$		$\overline{CK}$	VDD	CKE
H	NC	$\overline{CS}$	$\overline{WE}$		A10/AP	ZQ	NC
J	VSS	BA0	BA2		NC	VERFCA	VSS
K	VDD	A3	A0		A12/$\overline{BC}$	BA1	VDD
L	VSS	A 5	A2		A1	A4	VSS
M	VDD	A7	A9		A11	A6	VDD
N	VSS	$\overline{RESET}$	A13		NC	A8	VSS

x 8

Fig. 2: Pin Configuration — 96 balls BGA Package (X16)

< TOP View>

See the balls through the package

x 16

1	2	3		7	8	9
VDDQ	DQU5	DQU7	A	DQU4	VDDQ	VSS
VSSQ	VDD	VSS	B	$\overline{\text{DQSU}}$	DQU6	VSSQ
VDDQ	DQU3	DQU1	C	DQSU	DQU2	VDDQ
VSSQ	VDDQ	DMU	D	DQU0	VSSQ	VDD
VSS	VSSQ	DQL0	E	DML	VSSQ	VDDQ
VDDQ	DQL2	DQSL	F	DQL1	DQL3	VSSQ
VSSQ	DQL6	$\overline{\text{DQSL}}$	G	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQL4	H	DQL7	DQL5	VDDQ
NC	VSS	$\overline{\text{RAS}}$	J	CK	VSS	NC
ODT	VDD	$\overline{\text{CAS}}$	K	$\overline{\text{CK}}$	VDD	CKE
NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$	L	A10/AP	ZQ	NC
VSS	BA0	BA2	M	NC	VREFCA	VSS
VDD	A3	A0	N	A12/$\overline{\text{BC}}$	BA1	VDD
VSS	A 5	A2	P	A1	A4	VSS
VDD	A7	A9	R	A11	A6	VDD
VSS	$\overline{\text{RESET}}$	NC	T	NC	A8	VSS

Table 2: Input / Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE, (CKE0), (CKE1)	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$, ($\overline{CS0}$), ($\overline{CS1}$), ($\overline{CS2}$), ($\overline{CS3}$)	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM, (DMU, DML)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS /$\overline{TQDS}$ is enabled by Mode Register A11 setting in MR1
BA0 - BA2	Input	**Bank Address Inputs:** BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A10 / AP	Input	**Auto-Precharge**: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A0 – A13	Input	**Address Inputs:** Provide the row address for Activate commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional function as below.) The address inputs also provide the op-code during Mode Register Set commands.

Symbol	Type	Function
A12/$\overline{BC}$	Input	**Burst Chop:** A12/$\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
ODT, (ODT0), (ODT1)	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.
DQL, DQU, DQS,($\overline{DQS}$), DQSL,($\overline{DQSL}$), DQSU,($\overline{DQSU}$),	Input/output	**Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. The data strobes DQS, DQSL, DQSU are paired with differential signals $\overline{DQS}$, $\overline{DQSL}$, $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during both reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, ($\overline{TDQS}$)	Output	**Termination Data Strobe:** TDQS/$\overline{TDQS}$ is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11=0 in MR1, DM/$\overline{TDQS}$ will provide the data mask function and $\overline{TDQS}$ is not used. x16 DRAMs must disable the TDQS function via mode register A11=0 in MR1.
NC	-	**No Connect:** No internal electrical connection is present.
V$_{DDQ}$	Supply	**DQ Power Supply:** 1.5V ± 0.075V &1.35V -0.067/+0.1V
V$_{DD}$	Supply	**Power Supply:** 1.5V ± 0.075V &1.35V -0.067/+0.1V
V$_{SSQ}$	Supply	**DQ Ground**
V$_{ss}$	Supply	**Ground**
V$_{REFCA}$	Supply	**Reference voltage for CA**
V$_{REFDQ}$	Supply	**Reference voltage for DQ**
ZQ	Supply	**Reference pin for ZQ calibration.**

Note: Input only pins (BA0-BA2, A0-A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$) do not supply termination.

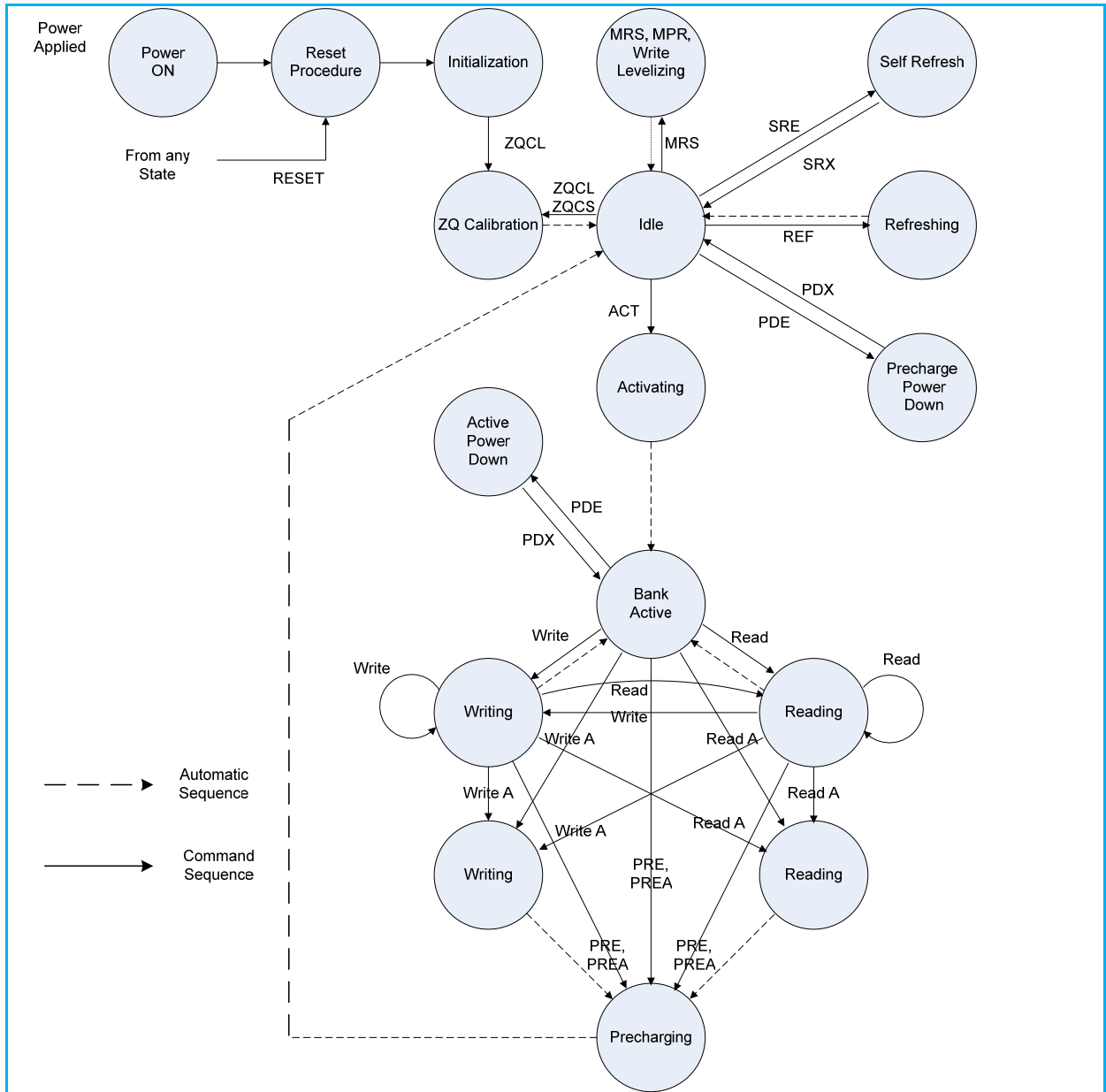# Fig. 3: Simplified State Diagram

Table 5: State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PED	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	$\overline{\text{RESET}}$	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A13 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

RESET and Initialization Procedure

Power-up Initialization sequence

The Following sequence is required for POWER UP and Initialization

1. Apply power ($\overline{\text{RESET}}$ is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200μs with stable power. CKE is pulled "Low" anytime before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD_{min} must be no greater than 200ms; and during the ramp, VDD>VDDQ and (VDD-VDDQ) <0.3 Volts.

- VDD and VDDQ are driven from a single power converter output, AND

- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND

- V_{ref} tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.

- Apply VDDQ without any slope reversal before or at the same time as VTT & V_{ref}.

- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clock (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (t_{IS}) must be meeting. Also a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of t_{DLLK} and t_{ZQinit}.

4. The DDR3 DRAM will keep its on-die termination in high impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the DRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. [tXPR=max (tXS, 5tCK)]

6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1)

7. Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1)

8. Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 and BA2)

9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-BA2)

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both t_{DLLK} and t_{ZQinit} completed.

12. The DDR3 SDRAM is now ready for normal operation.

Fig. 4: Reset and Initialization Sequence at Power- on Ramping (Cont'd)
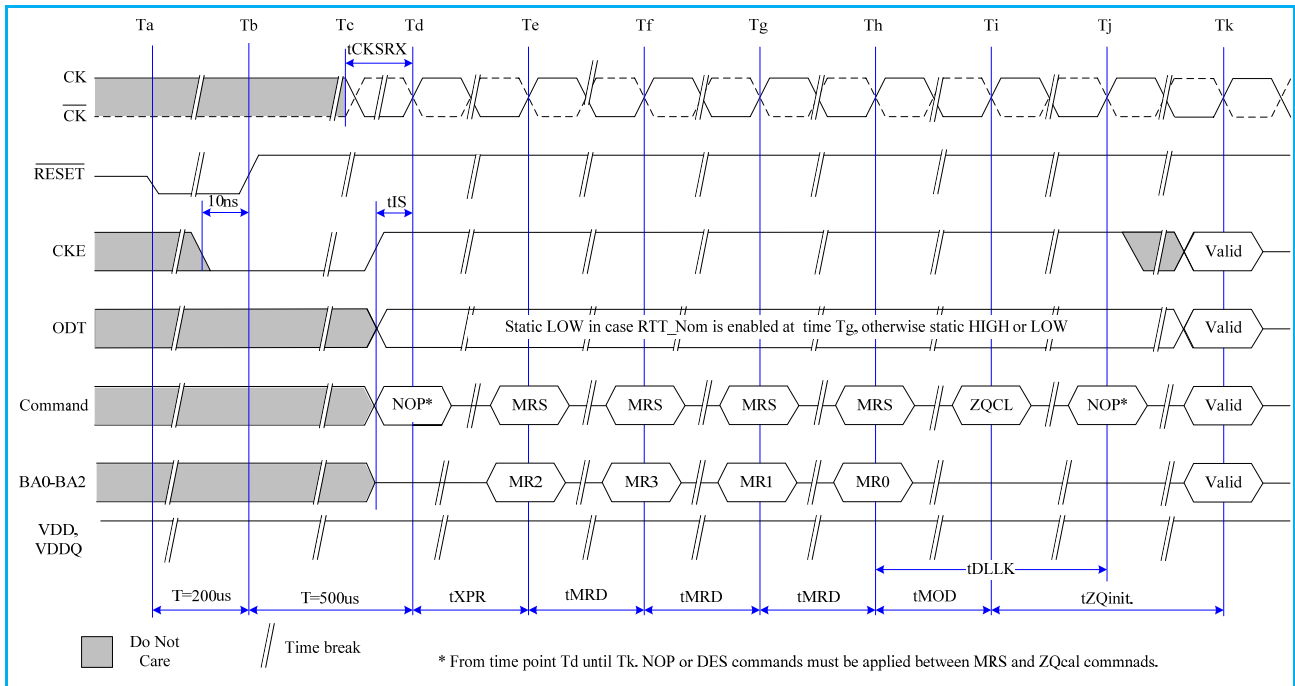

Reset Procedure at Stable Power (Cont'd)

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2*VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100ns. CKE is pulled "Low" before RESET being de-asserted (min. time 10ns).

2. Follow Power-up Initialization Sequence step 2 to 11.

3. The Reset sequence is now completed. DDR3 SDRAM is ready for normal operation.

## Fig. 5: Reset Procedure at Power Stable Condition
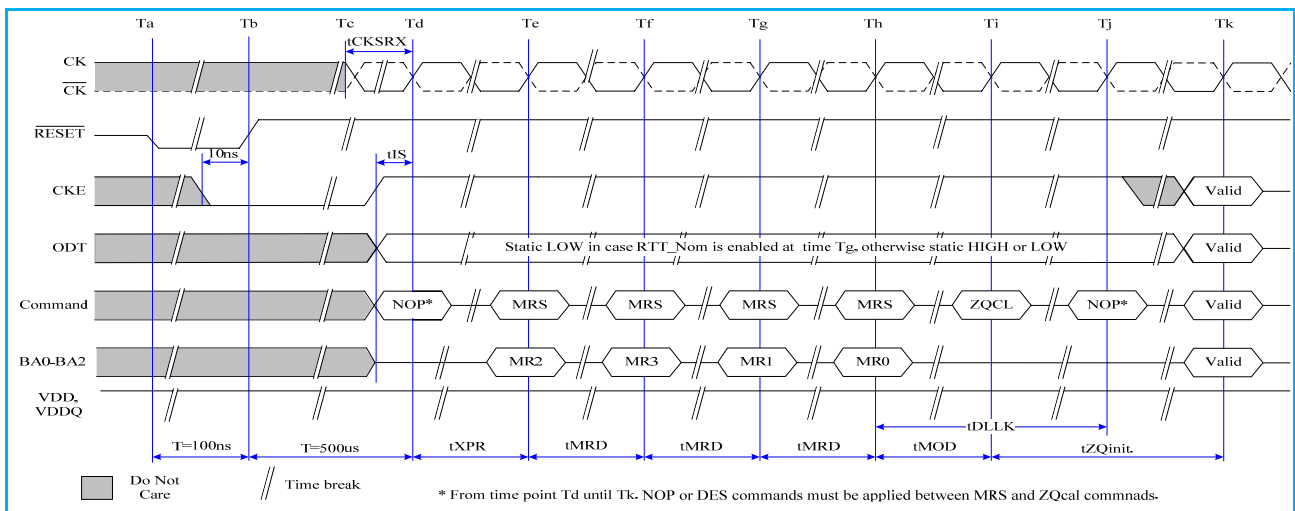
Register Definition
Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers ($\overline{MR}$) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, t_{MRD} is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown as below.

Fig. 6: t_{MRD} Timing
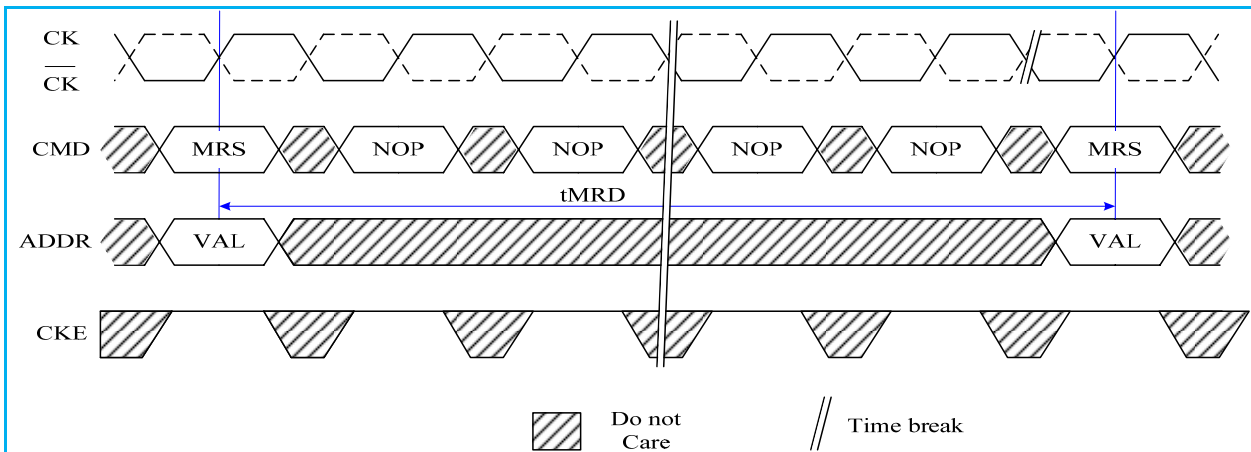
The MRS command to Non-MRS command delay, tMOD, is require for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown as the following figure.

Fig. 7: t~MOD~ Timing
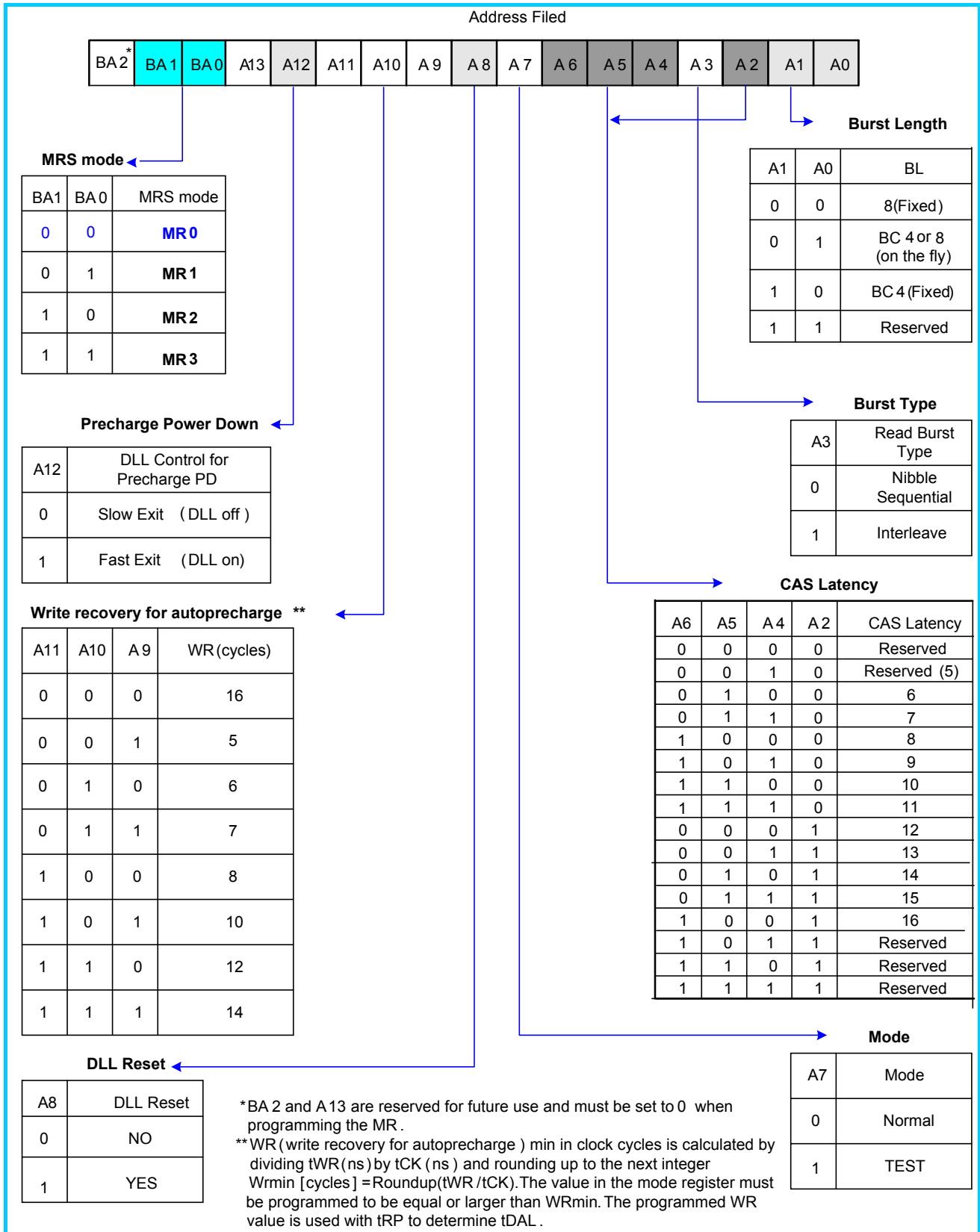
Fig. 7: t_{MOD} Timing
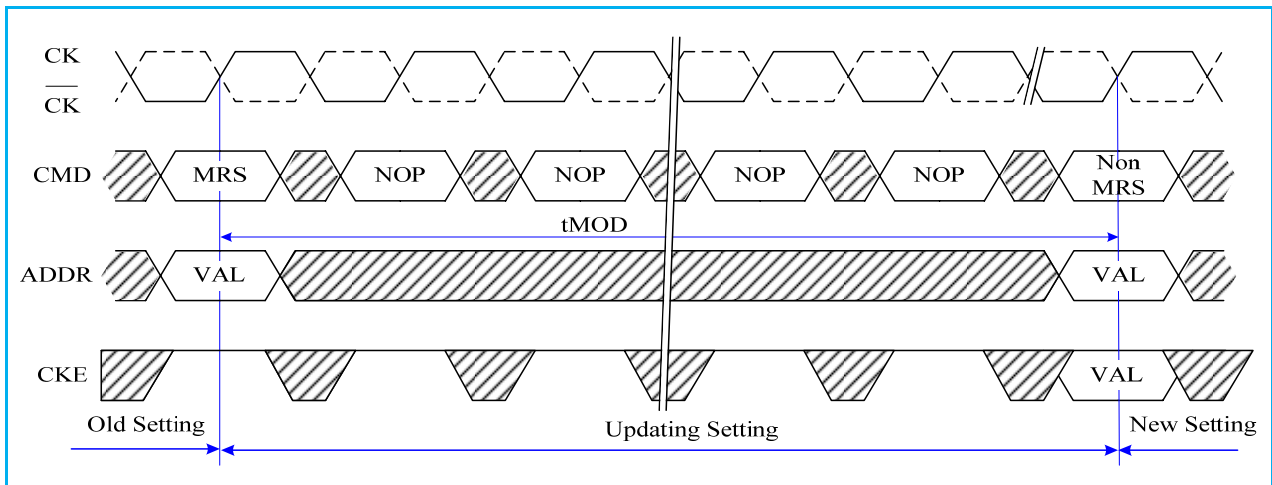
Programming the Mode Registers (Cont'd)

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

Mode Register MR0

The mode-register MR0 stores data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

Fig. 8:MR0 Definition

Address Filed

| BA 2 * | BA 1 | BA 0 | A13 | A12 | A11 | A10 | A 9 | A 8 | A 7 | A 6 | A 5 | A 4 | A 3 | A 2 | A1 | A0 |

MRS mode

BA1	BA 0	MRS mode
0	0	**MR 0**
0	1	**MR 1**
1	0	**MR 2**
1	1	**MR 3**

Precharge Power Down

A12	DLL Control for Precharge PD
0	Slow Exit （DLL off)
1	Fast Exit （DLL on)

**Write recovery for autoprecharge ** **

A11	A10	A 9	WR (cycles)
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

DLL Reset

A8	DLL Reset
0	NO
1	YES

Burst Length

A1	A0	BL
0	0	8 (Fixed)
0	1	BC 4 or 8 (on the fly)
1	0	BC 4 (Fixed)
1	1	Reserved

Burst Type

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

CAS Latency

A6	A5	A 4	A 2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	Reserved (5)
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14
0	1	1	1	15
1	0	0	1	16
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

Mode

A7	Mode
0	Normal
1	TEST

*BA 2 and A 13 are reserved for future use and must be set to 0 when programming the MR .

**WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer Wrmin [cycles] = Roundup(tWR /tCK).The value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL .

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/$\overline{BC}$.

Table 6: Burst Type and Burst Order

Burst Length	Read Write	Starting Column Address (A2,A1,A0)	Burst type: Sequential (decimal) A3 = 0	Burst type: Interleaved (decimal) A3 = 1	Note
4 Chop	Read	0 , 0 , 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 , 0 , 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	
		0 , 1 , 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	
		0 , 1 , 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	
		1 , 0 , 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	
		1 , 0 , 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	
		1 , 1 , 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	
		1 , 1 , 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	
	Write	0 , V , V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1 , V , V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	
8	Read	0 , 0 , 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 , 0 , 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	
		0 , 1 , 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	
		0 , 1 , 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	
		1 , 0 , 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	
		1 , 0 , 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	
		1 , 1 , 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	
		1 , 1 , 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	
	Write	V , V , V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

Note:
1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/$\overline{BC}$, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0~7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Do not Care.

CAS Latency

The CAS Latency is defined by MR0 (bit A9~A11) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0 (bit7=0) and all other bits set to the desired values shown in the MR0 definition figure. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should not be used. No operations or functionality is guaranteed if A7=1.

DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

Write Recovery

The programmed WR value MR0(bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR (write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(ns) by tCK(ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal or larger than tWR (min).
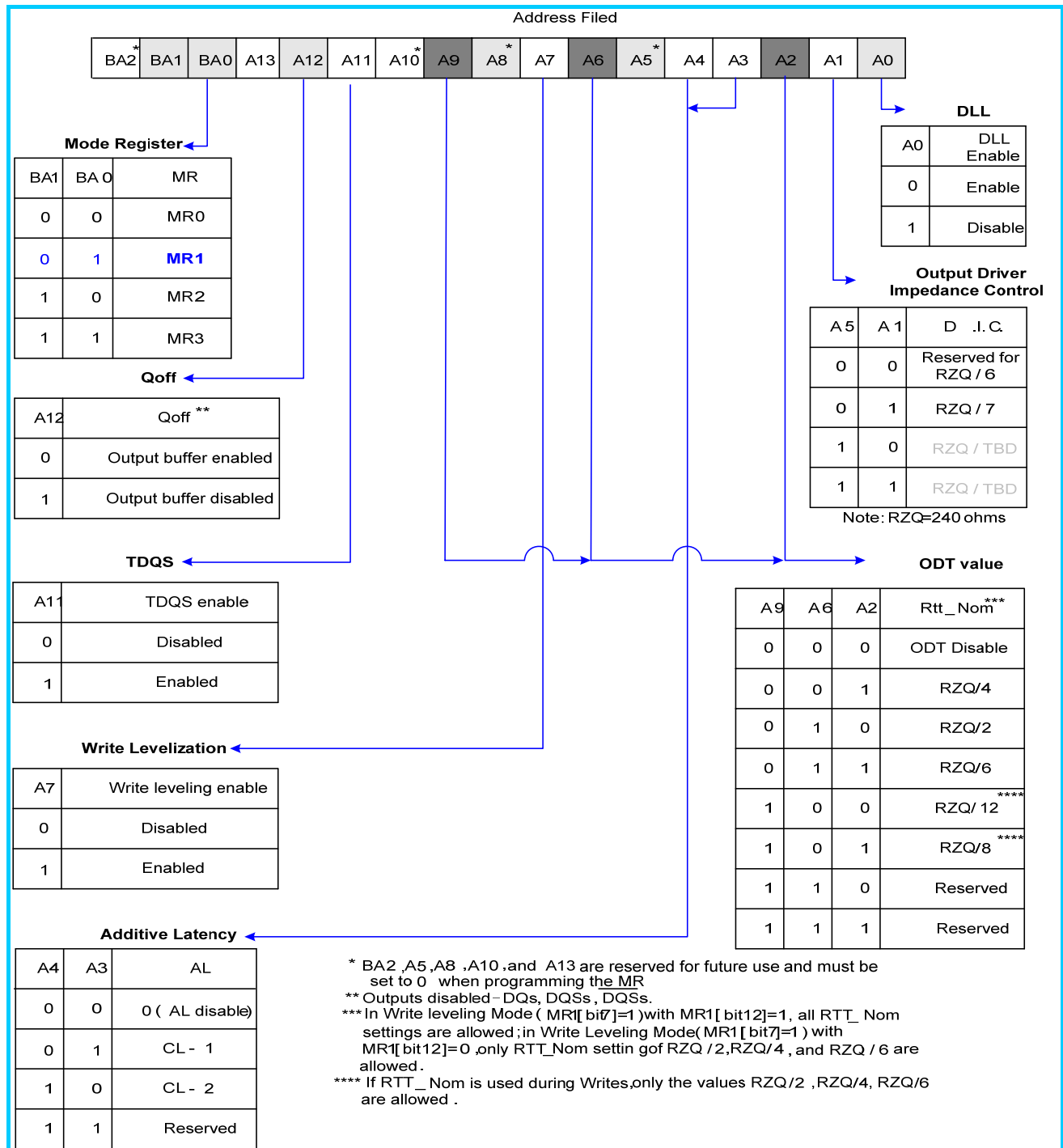
Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output strength, Rtt_Nom impedance, additive latency, WRITE leveling enable and Qoff. The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the following figure.

Fig. 9: MR1 Definition

Mode Register

BA1	BA 0	MR
0	0	MR0
0	1	**MR1**
1	0	MR2
1	1	MR3

Qoff

A12	Qoff**
0	Output buffer enabled
1	Output buffer disabled

TDQS

A11	TDQS enable
0	Disabled
1	Enabled

Write Levelization

A7	Write leveling enable
0	Disabled
1	Enabled

Additive Latency

A4	A3	AL
0	0	0 (AL disable)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

DLL

A0	DLL Enable
0	Enable
1	Disable

Output Driver Impedance Control

A5	A 1	D .I.C.
0	0	Reserved for RZQ / 6
0	1	RZQ / 7
1	0	RZQ / TBD
1	1	RZQ / TBD

Note: RZQ=240 ohms

ODT value

A 9	A 6	A 2	Rtt_Nom***
0	0	0	ODT Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/ 12****
1	0	1	RZQ/8****
1	1	0	Reserved
1	1	1	Reserved

* BA2 ,A5 ,A8 ,A10 ,and A13 are reserved for future use and must be set to 0 when programming the MR
** Outputs disabled – DQs, DQSs , DQSs.
*** In Write leveling Mode (MR1[bit7]=1)with MR1[bit12]=1, all RTT_ Nom settings are allowed ; in Write Leveling Mode(MR1[bit7]=1) with MR1[bit12]=0 ,only RTT_Nom settin gof RZQ / 2,RZQ/4 , and RZQ / 6 are allowed .
**** If RTT_ Nom is used during Writes,only the values RZQ/2 ,RZQ/4, RZQ/6 are allowed .

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0=0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enable upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, expect when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation in DLL-off Mode.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0, 0}, to disable Dynamic ODT externally.

Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1(bit A1 and A5) as shown in MR1 definition figure.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmable in MR1. A separate value (Rtt_WR) may be programmable in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown as the following table.

Table 7: Additive Latency (AL) Settings

A4	A3	AL
0	0	0, (AL Disable)
0	1	CL-1
1	0	CL-2
1	1	Reserved

Write leveling

For better signal integrity, DDR3 memory module adopted fly by topology for the commands, addresses, control signals, and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate for skew.

Output Disable

The DDR3 SDRAM outputs maybe enable/disabled by MR1 (bit12) as shown in MR1 definition. When this feature is enabled (A12=1) all output pins (DQs, DQS, $\overline{DQS}$, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring modules power for example. For normal operation A12 should be set to '0'.

TDQS, $\overline{TDQS}$

TDQS (Termination Data Strobe) is a feature of x8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

When enabled via the mode register, the same termination resistance function is applied to be TDQS/$\overline{TDQS}$ pins that are applied to the DQS/$\overline{DQS}$ pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the $\overline{TDQS}$ pin is not used.

The TDQS function is available in x8 DDR3/L SDRAM only and must be disabled via the mode register A11=0 in MR1 for x16 configurations.

Table 8: TDQS, $\overline{TDQS}$ Function Matrix

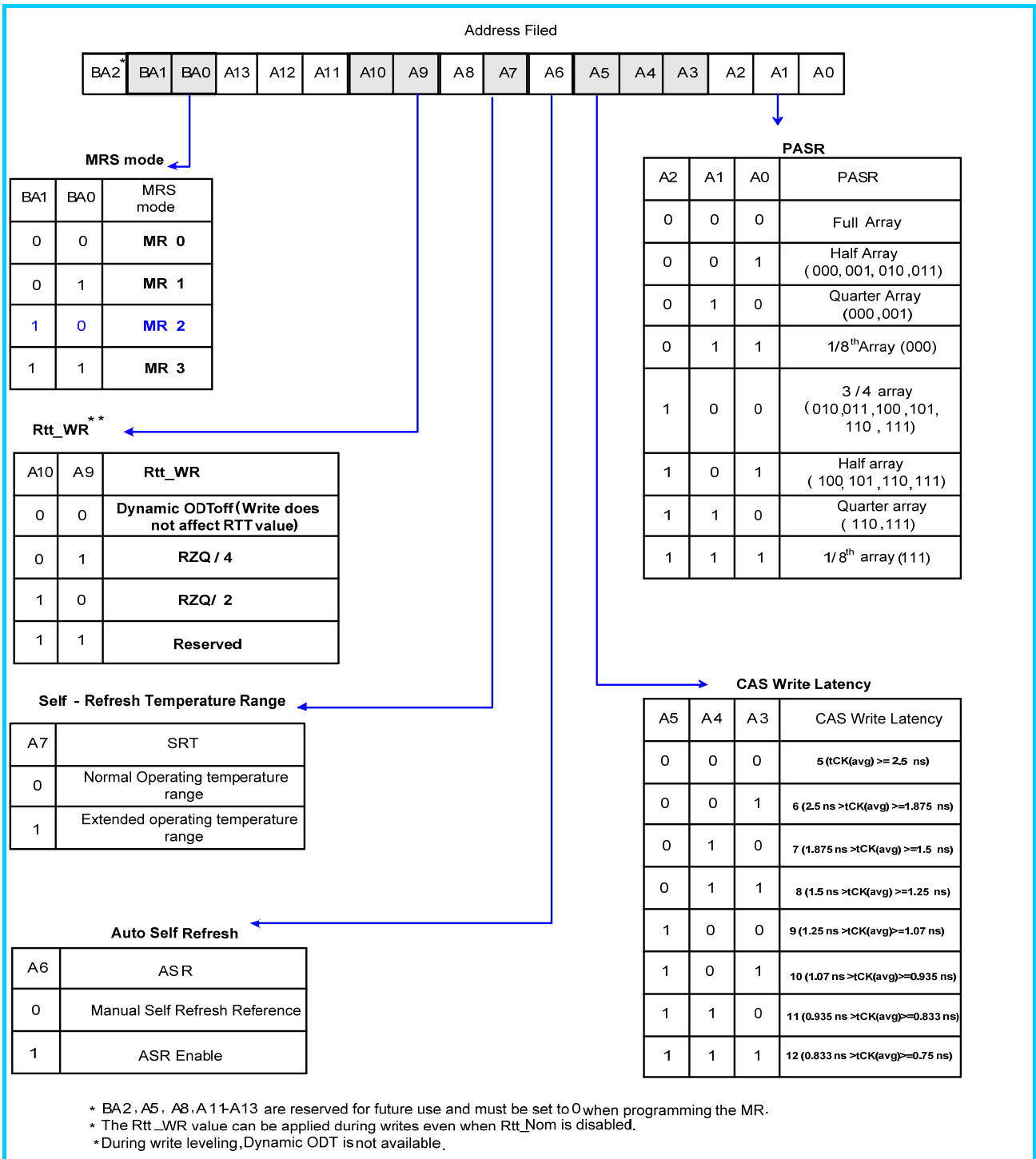| MR1 (A11)	DM / TDQS	NU / TDQS
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	$\overline{TDQS}$
Note:		
1. If TDQS is enabled, the DM function is disabled.		
2. When not used, TDQS function can be disabled to save termination power.		
3. TDQS function is only available for x8 DRAM and must be disabled for x16.		

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

Fig. 10: MR2 Definition

Address Filed

| BA2* | BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

MRS mode

BA1	BA0	MRS mode
0	0	**MR 0**
0	1	**MR 1**
1	0	**MR 2**
1	1	**MR 3**

PASR

A2	A1	A0	PASR
0	0	0	Full Array
0	0	1	Half Array (000, 001, 010 ,011)
0	1	0	Quarter Array (000 ,001)
0	1	1	1/8th Array (000)
1	0	0	3 / 4 array (010,011,100 ,101, 110 , 111)
1	0	1	Half array (100, 101 ,110 ,111)
1	1	0	Quarter array (110 ,111)
1	1	1	1/ 8th array (111)

Rtt_WR **

A10	A9	Rtt_WR
0	0	**Dynamic ODToff (Write does not affect RTT value)**
0	1	**RZQ / 4**
1	0	**RZQ/ 2**
1	1	**Reserved**

CAS Write Latency

A5	A4	A3	CAS Write Latency
0	0	0	5 (tCK(avg) >= 2.5 ns)
0	0	1	6 (2.5 ns >tCK(avg) >=1.875 ns)
0	1	0	7 (1.875 ns >tCK(avg) >=1.5 ns)
0	1	1	8 (1.5 ns >tCK(avg) >=1.25 ns)
1	0	0	9 (1.25 ns >tCK(avg)>=1.07 ns)
1	0	1	10 (1.07 ns >tCK(avg)>=0.935 ns)
1	1	0	11 (0.935 ns >tCK(avg)>=0.833 ns)
1	1	1	12 (0.833 ns >tCK(avg)>=0.75 ns)

Self - Refresh Temperature Range

A7	SRT
0	Normal Operating temperature range
1	Extended operating temperature range

Auto Self Refresh

A6	ASR
0	Manual Self Refresh Reference
1	ASR Enable

* BA2, A5, A8, A11-A13 are reserved for future use and must be set to 0 when programming the MR.
* The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.
* During write leveling, Dynamic ODT is not available.

CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL=AL+CWL.

For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on page116. For detailed Write operation refer to "WRITE Operation" on page41.

Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

DDR3 SDRAM must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3/L SDRAM devices support the following options or requirements referred to in this material. For more details refer to "Extended Temperature Usage" on page41. DDR3 SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings.

DDR3/L SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3/L SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to "Dynamic ODT" on page69.

Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

Fig. 11: MR3 Definition

Address Filed

| BA2 | BA 1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A 7 | A6 | A5 | A4 | A3 | A2 | A 1 | A0 |

MRS mode

BA 1	BA 0	MRS mode
0	0	**MR 0**
0	1	**MR1**
1	0	**MR2**
1	1	**MR3**

MPR Location

A1	A0	MPR Location
0	0	PredefinedPattern[2]*
0	1	RFU
1	0	RFU
1	1	RFU

MPR Operation

A2	MPR
0	Normal Operation
1	Dataflow fromMPR

Note：BA2, A3-A13 are reserved for future use and mustbe set to 0 when programming the MR.
The predefined pattern will be used for read synchronization.
When MPR control is set for normal operation (MR3 A[2] =0) then MR3 A[1:0] will be ignored.

Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a Mode Register Set (MRS) command must be issued to MR3 register with bit A2=1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2=0). Power down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence.

Fig. 12: MPR Block Diagram
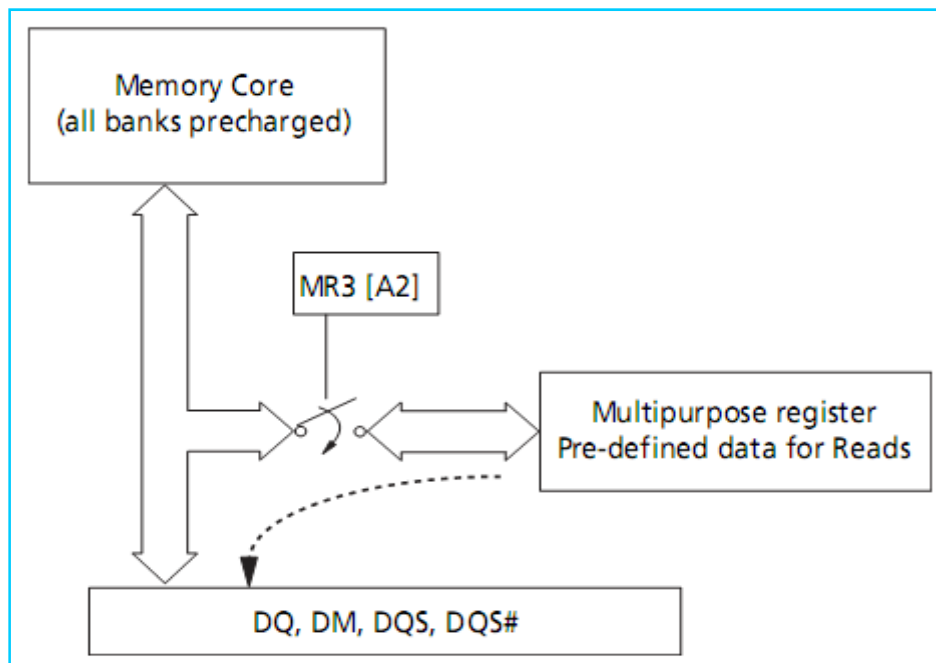
To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as following Table 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown on page28. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Table 9: MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See the page28	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

MPR Functional Description

•One bit wide logical interface via all DQ pins during READ operation.

•Register Read on x8:

•DQ[0] drives information from MPR.

•DQ[7:1] either drive the same information as DQ [0], or they drive 0b.

•Register Read on x16:

•DQL[0] and DQU[0] drive information from MPR.

•DQL[7:1] and DQU[7:1] either drive the same information as DQL [0], or they drive 0b.

•Addressing during for Multi Purpose Register reads for all MPR agents:

•BA [2:0]: don't care

•A[1:0]: A[1:0] must be equal to '00'b. Data read burst order in nibble is fixed

•A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst

Chop 4 cases, the burst order is switched on nibble base A [2]=0b, Burst order: 0,1,2,3 *)

A[2]=1b, Burst order: 4,5,6,7 *)

•A[9:3]: don't care

•A10/AP: don't care

•A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.

•A11, A13,... (if available): don't care

•Regular interface functionality during register reads:

•Support two Burst Ordering which are switched with A2 and A[1:0]=00b.

•Support of read burst chop (MRS and on-the-fly via A12/BC)

•All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.

•Regular read latencies and AC timings apply.

•DLL must be locked prior to MPR Reads.

NOTE: *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

Table 10: MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Predefined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7

NOTE: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

DDR3 SDRAM Command Description and Operation
Table 11: Command Truth Table

Function	Abbreviation	CKE Previous Cycle	CKE Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-BA2	A13-$\overline{A15}$	A12-$\overline{BC}$	A10-$\overline{AP}$	A0-9, $\overline{A11}$	NOTES
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

DDR3 SDRAM Command Description and Operation

Command Truth Table (Conti.)

NOTE1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

NOTE2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

NOTE5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE6. The Power-Down Mode does not perform any refresh operation.

NOTE7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE8. Self Refresh Exit is asynchronous.

NOTE9. VREF (Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.

NOTE10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.

NOTE11. The Deselect command performs the same function as No Operation command.

NOTE12. Refer to the CKE Truth Table for more detail with CKE transition.

Table 12: CKE Truth Table

Current State	CKE Previous Cycle (N-1)	CKE Current Cycle (N)	Command (N) $\overline{RAS}, \overline{CAS}, \overline{WE}, \overline{CS}$	Action (N)	Notes
Power-Down	L	L	X	Maintain Power-Down	
	L	H	DESELECT or NOP	Power-Down Exit	
Self-Refresh	L	L	X	Maintain Self-Refresh	
	L	H	DESELECT or NOP	Self-Refresh Exit	
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	
Reading	H	L	DESELECT or NOP	Power-Down Entry	
Writing	H	L	DESELECT or NOP	Power-Down Entry	
Precharging	H	L	DESELECT or NOP	Power-Down Entry	
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	
	H	L	REFRESH	Self-Refresh	

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registrations. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh modes can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are NOP and DESELECT only.

NOTE 13 Self-Refresh cannot be entered during Read or Write operations.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15 "X" means "don't care"(including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

NOTE 18 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

No Operation (NOP) Command

The No operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP ($\overline{CS}$ low and $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Deselect Command

The Deselect function ($\overline{CS}$ HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3/L SDRAM is effectively deselected. Operations already in progress are not affected.

DLL- Off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this   will disable the DLL for subsequent operations until A0 bit set back to "0". The MR1 A0 bit for DLL control can be switched either during initialization or later.

The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK) but not the data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL-1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation have shown at the following Timing Diagram (CL=6, BL=8)

Fig. 13 DLL-off mode READ Timing Operation
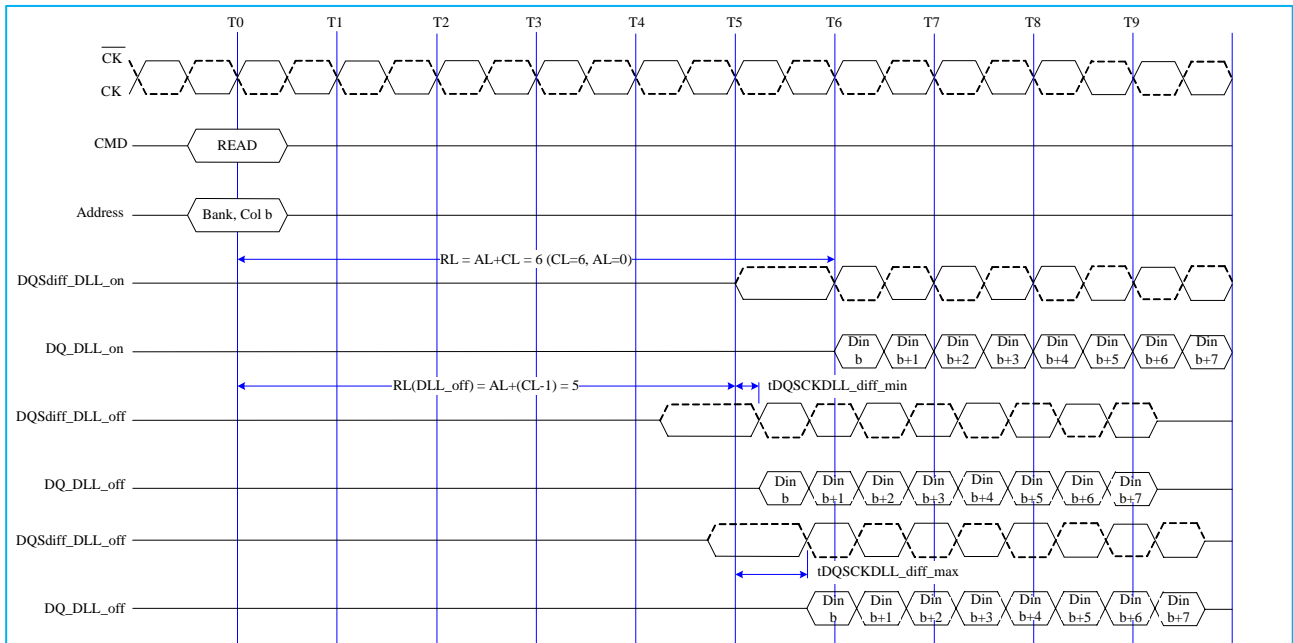
Note: The tDQSCK is used here for DQS, DQS, and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ, DQS, and $\overline{DQS}$ signals will still be tDQSQ.

DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operation until A0 bit set back to "0".

DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh outlined in the following procedure:

1. Starting from Idle state (all banks pre-charged, all timing fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL).

2. Set MR1 Bit A0 to "1" to disable the DLL.

3. Wait tMOD.

4. Enter Self Refresh Mode; wait until (tCKSRE) satisfied.

5. Change frequency, in guidance with "Input Clock Frequency Change" section.

6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.

8. Wait tXS, and then set Mode Registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. A ZQCL command may also be issued after tXS).

9. Wait for tMOD, and then DRAM is ready for next command.

Fig. 14: DLL Switch Sequence from DLL-on to DLL-off

Note:
ODT: Static LOW in case RTT_Nom and RTT_WR is enabled, otherwise static Low or High
1) Starting with Idle State, RTT in Hi-Z State.
2) Disable DLL by setting MR1 Bit A0 to 1.
3) Enter SR.
4) Change Frequency.
5) Clock must be stable at least tCKSRX.
6) Exit SR.
7) Update Mode registers with DLL off parameters setting.
8) Any valid command.
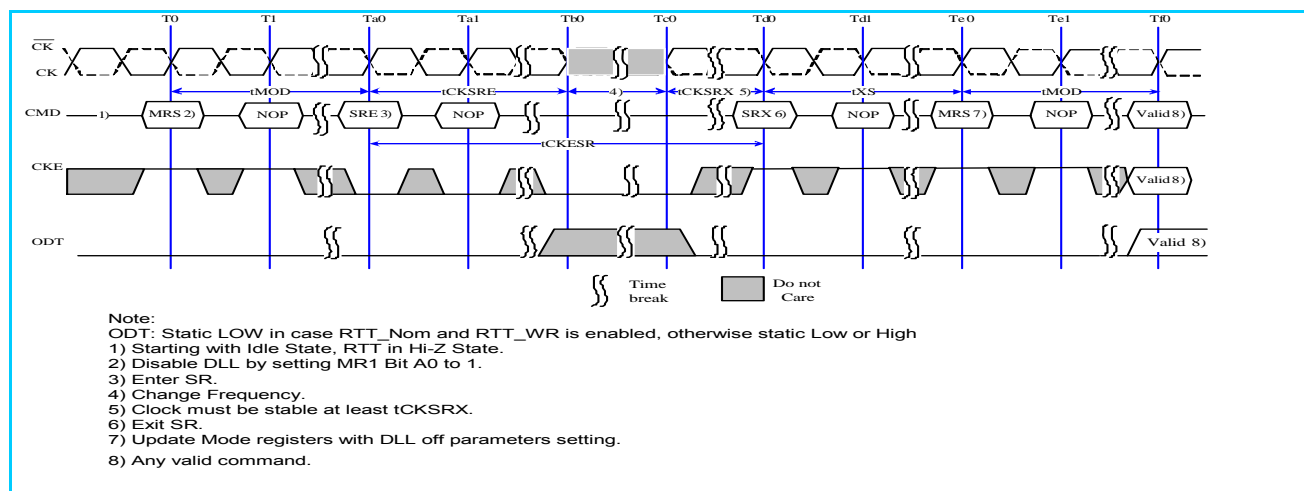
DLL "off" to DLL "on" Procedure

To switch from DLL "off" to DLL "on" (with requires frequency change) during Self-Refresh:

1. Starting from Idle state (all banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered).

2. Enter Self Refresh Mode, wait until tCKSRE satisfied.

3. Change frequency, in guidance with "Input clock frequency change" section.

4. Wait until a stable is available for at least (tCKSRX) at DRAM inputs.

5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered. the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.

6. Wait tXS, then set MR1 Bit A0 to "0" to enable the DLL.

7. Wait tMRD, then set MR0 Bit A8 to "1" to start DLL Reset.

8. Wait tMRD, then set Mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK).

9. Wait for tMOD, then DRAM is ready for next command (remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.

Fig. 15 DLL Switch Sequence from DLL-on to DLL-off

Note:
ODT: Static LOW in case RTT_Nom and RTT_WR is enabled, otherwise static Low or High
1) Starting from Idle State.
2) Enter SR.
3) Change Frequency.
4) Clock must be stable at least tCKSRX.
5) Exit SR.
6) Set DLL-on by MR1 A0="0"
7) Start DLL Reset
8) Any valid command
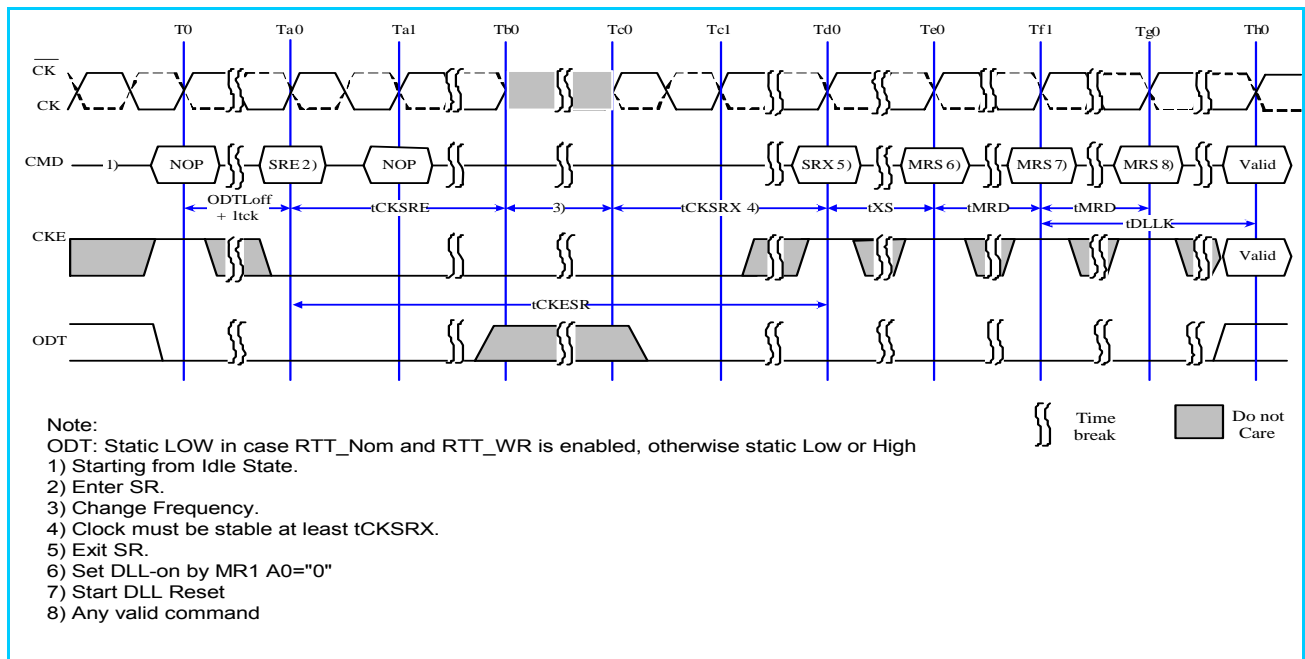
Input Clock frequency change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specification.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-Down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode of the sole purpose of changing the clock frequency. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade.

The second condition is when the DDR3 SDRAM is in Precharge Power-Down mode (either fast exit mode or slow exit mode). If the RTT_Nom feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_Nom feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3/L SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before precharge Power Down may be exited; after Precharge Power Down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

## Fig. 16: Change Frequency during Precharge Power-down
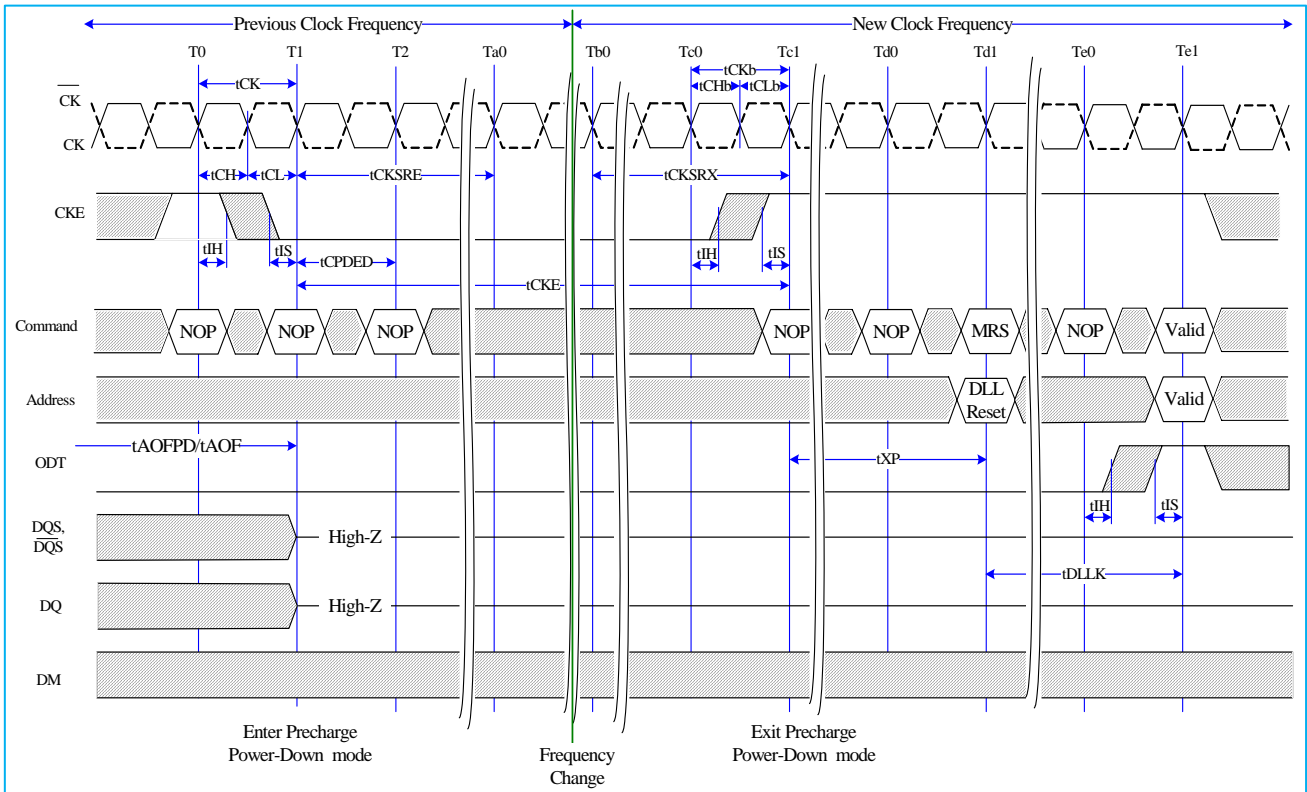
NOTES:

1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down

2. tAOFPD and tAOF must be statisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements

3. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT

signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register

prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in

this case.

Write Leveling

For better signal integrity, DDR3 memory adopted fly by topology for the commands, addresses, control signals, and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support "write leveling" in DDR3 SDRAM to compensate the skew.

The memory controller can use the "write leveling" feature and feedback from the DDR3 SDRAM to adjust the DQS - $\overline{DQS}$ to CK - $\overline{CK}$ relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - $\overline{DQS}$ to align the rising edge of DQS - $\overline{DQS}$ with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK - $\overline{CK}$, sampled with the rising edge of DQS - $\overline{DQS}$, through the DQ bus. The controller repeatedly delays DQS - $\overline{DQS}$ until a transition from 0 to 1 is detected. The DQS - $\overline{DQS}$ delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS, and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS- $\overline{DQS}$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in "AC Timing Parameters" section in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is show as below figure.

Fig. 17: Write Leveling Concept
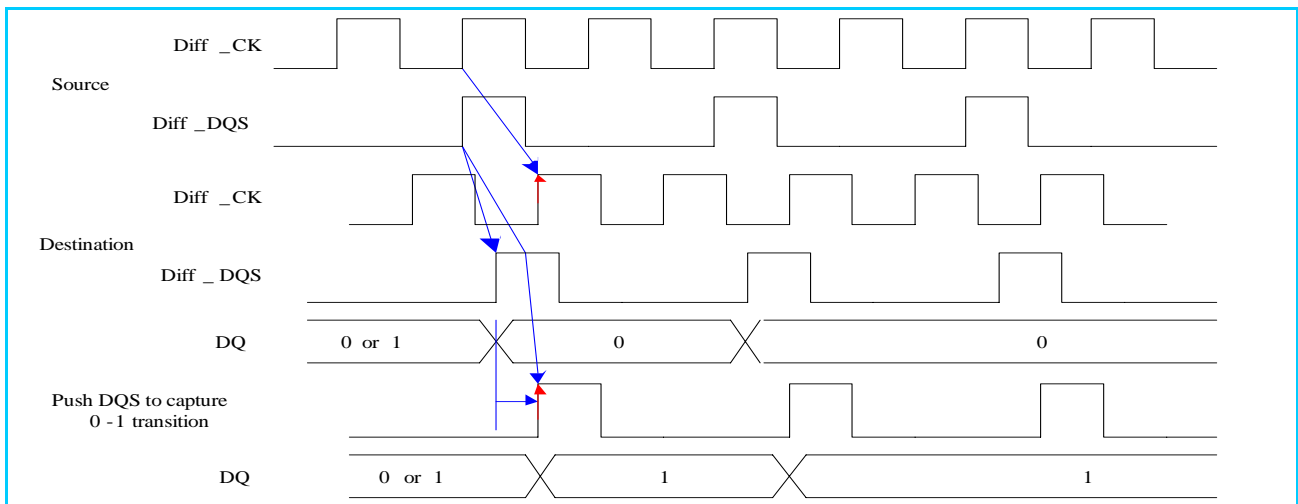
DQS/$\overline{DQS}$ driven by the controller during leveling mode must be determined by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations x8. Therefore, a separate feedback mechanism should be able for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS (diff_LDQS) to clock relationship.

DRAM setting for write leveling and DRAM termination unction in that mode

DRAM enters into Write leveling mode if A7 in MR1 set "High" and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set "Low". Note that in write leveling mode, only DQS/$\overline{DQS}$ terminations are activated and deactivated via ODT pin not like normal operation.

Table 13: MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

Table 14: DRAM termination function in the leveling mode

ODT pin at DRAM	DQS/$\overline{DQS}$ termination	DQs termination
De-asserted	off	off
Asserted	on	off

Note: In write leveling mode with its output buffer disabled (MR1[bit7]=1 with MR1[bit12]=1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7]=1 with MR1[bit12]=0) only RTT_Nom settings of RZQ/2, RZQ/4, and RZQ/6 are allowed.

Procedure Description

Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or Deselect commands are allowed. As well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other rank must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.

Controller may drive DQS low and $\overline{DQS}$ high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD controller provides a single DQS, $\overline{DQS}$ edge which is used by the DRAM to sample CK – $\overline{CK}$ driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - $\overline{CK}$ status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS/DQS) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS – $\overline{DQS}$ delay setting and launches the next DQS/$\overline{DQS}$ pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS – $\overline{DQS}$ delay setting and write leveling is achieved for the device. The following figure describes the timing diagram and parameters for the overall Write leveling procedure.

Absolute Maximum Ratings

Table 25: Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pin relative to Vss	-0.4 ~ 1.975	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.975	V	1,3
Vin, Vout	Voltage on any pin relative to Vss	-0.4 ~ 1.975	V	1
Tstg	Storage Temperature	-55 ~ 100	°C	1,2

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.

3. VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6VDDQ, when VDD and VDDQ are less than 500mV; Vref may be equal to or less than 300mV.

Table 26: Temperature Range

Symbol	Condition	Parameter	Value	Units	Notes
Toper	Commercial	Normal Operating Temperature Range	0 to 85	°C	1,2
		Extended Temperature Range	85 to 95	°C	1,3
	Industrial	Operating Temperature Range	-40 to 95	°C	1.4

Note:

1. Operating Temperature Toper is the case surface temperature on the center/top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specification will be supported.

During   operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional apply.

a)   Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1x refresh (tREFI to 7.8us) in the Extended Temperature Range.

b)   If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

4. During Industrial Temperature Operation Range, the DRAM case temperature must be maintained between -40°C~95°C under all operating Conditions.

AC & DC Operating Conditions

Table 27: Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min.	Typ.	Max.		
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3. Maximun DC value may not be great than 1.425V.The DC value is the linear average of VDD/ VDDQ(t) over a very long period of time

(e.g., 1 sec).

4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.

AC & DC Input Measurement Levels

Table 28: AC and DC Logic Input Levels for Single-Ended Signals & Command and Address

Symbol	Parameter	DDR3-1066/1333				Unit	Note
		Min.	Max.				
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD			V	1,5
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100			V	1,6
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note2			V	1,2,7
VIL.CA(AC175)	AC input logic low	Note2	Vref - 0.175			V	1,2,8
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note2			V	1,2,7
VIL.CA(AC150)	AC input logic low	Note2	Vref - 0.150			V	1,2,8
VIH.CA(AC135)	AC input logic high	-	-			V	1,2,7
VIL.CA(AC135)	AC input logic low	-	-			V	1,2,8
VIH.CA(AC125)	AC input logic high	-	-			V	1,2,7
VIL.CA(AC125)	AC input logic low	-	-			V	1,2,8
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD			V	3,4

Note:

NOTE **1.** For input only pins except RESET.Vref=VrefCA(DC)

NOTE **2.** See "Overshoot and Undershoot Specifications"

NOTE **3.** The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 0.1% VDD.

NOTE **4.** For reference: approx. VDD/2 +/- 15mv, DDR3L is VDD/2 +/-13.5mv.

NOTE **5**. VIH(dc) is used as a simplified symbol for VIH.CA(DC100)

NOTE **6**. VIL(dc) is used as a simplified symbol for VIL.CA(DC100)

NOTE **7**. VIH(ac) is used as a simplified symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135), and

VIH.CA(AC125); VIH.CA(AC175) value is used when Vref + 0.175V is referenced, VIH.CA(AC150)

value is used when Vref + 0.150V is referenced, VIH.CA(AC135) value is used when Vref + 0.135V is

referenced, and VIH.CA(AC125) value is used when Vref + 0.125V is referenced.

NOTE **8**. VIL(ac) is used as a simplified symbol for VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135) and

VIL.CA(AC125); VIL.CA(AC175) value is used when Vref - 0.175V is referenced, VIL.CA(AC150)

value is used when Vref - 0.150V is referenced, VIL.CA(AC135) value is used when Vref - 0.135V is

referenced, and VIL.CA(AC125) value is used when Vref - 0.125V is referenced.

Table 29: AC and DC Logic Input Levels for Single-Ended Signals & DQ and DM

Symbol	Parameter	DDR3-1066		DDR3-1333				Unit	Note
		Min.	Max.	Min.	Max.				
VIH.DQ(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD			V	1,5
VIL.DQ(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref – 0.100			V	1,6
VIH.DQ(AC175)	AC input logic high	Vref + 0.175	Note2	Vref + 0.150	Note2	-	-	V	1,2,7,9
VIL.DQ(AC175)	AC input logic low	Note2	Vref - 0.175	Note2	Vref – 0.150	-	-	V	1,2,8,9
VIH.DQ(AC150)	AC input logic high	Vref + 0.150	Note2	Vref + 0.150	Note2	-	-	V	1,2,7,9
VIL.DQ(AC150)	AC input logic low	Note2	Vref - 0.150	Note2	Vref – 0.150	-	-	V	1,2,8,9
VIH.DQ(AC135)	AC input logic high	-	-	-	-			mV	1,2,7
VIL.DQ(AC135)	AC input logic low							mV	1,2,8
VREFDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD			V	3,4

Note:

NOTE **1.** For input only pins except RESET.Vref=VrefCA(DC)

NOTE **2.** See "Overshoot and Undershoot Specifications"

NOTE **3.** The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 0.1% VDD.

NOTE **4.** For reference: approx. VDD/2 +/- 15mv

NOTE **5**. VIH(dc) is used as a simplified symbol for VIH.CA(DC100)

NOTE **6**. VIL(dc) is used as a simplified symbol for VIL.CA(DC100)

NOTE **7**. VIH(ac) is used as a simplified symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135), and

VIH.CA(AC125); VIH.CA(AC175) value is used when Vref + 0.175V is referenced, VIH.CA(AC150)

value is used when Vref + 0.150V is referenced, VIH.CA(AC135) value is used when Vref + 0.135V is

referenced, and VIH.CA(AC125) value is used when Vref + 0.125V is referenced.

NOTE **8**. VIL(ac) is used as a simplified symbol for VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135) and

VIL.CA(AC125); VIL.CA(AC175) value is used when Vref - 0.175V is referenced, VIL.CA(AC150)

value is used when Vref - 0.150V is referenced, VIL.CA(AC135) value is used when Vref - 0.135V is

referenced, and VIL.CA(AC125) value is used when Vref - 0.125V is referenced.

NOTE **9.** These levels apply for 1.35 Volt operation only. If the device is operated at 1.5V, the respective levels in

JESD79-3.(VIH/L.CA(DC100),VIH/L.CA (AC175), VIH/L.CA (AC150), etc.) apply. The 1.5V levels (VIH/L.CA (DC100), VIH/L.CA (AC175),

VIH/L.CA (AC150), etc.) do not apply when the device is operated in the 1.35Voltage range.

Table 30: AC and DC Logic Input Levels for Differential Signals

| Symbol | Parameter | DDR3-1066, 1333 | | Unit | Notes |
		Min.	Max.		
V_{IHdiff}	Differential input logic high	+0.200	Note3	V	1
V_{ILdiff}	Differential input logic low	Note3	-0.200	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (VIH(ac) – Vref)	Note3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	Note3	2 x (Vref - VIL(ac))	V	2

Note:

1. Used to define a differential signal slew-rate.

2. For CK - CK use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS, DQSL, DQSL, DQSU, DQSU use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also there.

3. These values are not defined, however the single-ended signals CK, CK, DQS, DQS, DQSL, DQSL, DQSU, DQSU need to be within the respective limits (VIH(dc)max, VIL(dc)min) for single-ended signals as well as limitations for overshoot and undershoot.

Fig. 62: Definition of differential ac-swing and "time above ac-level"
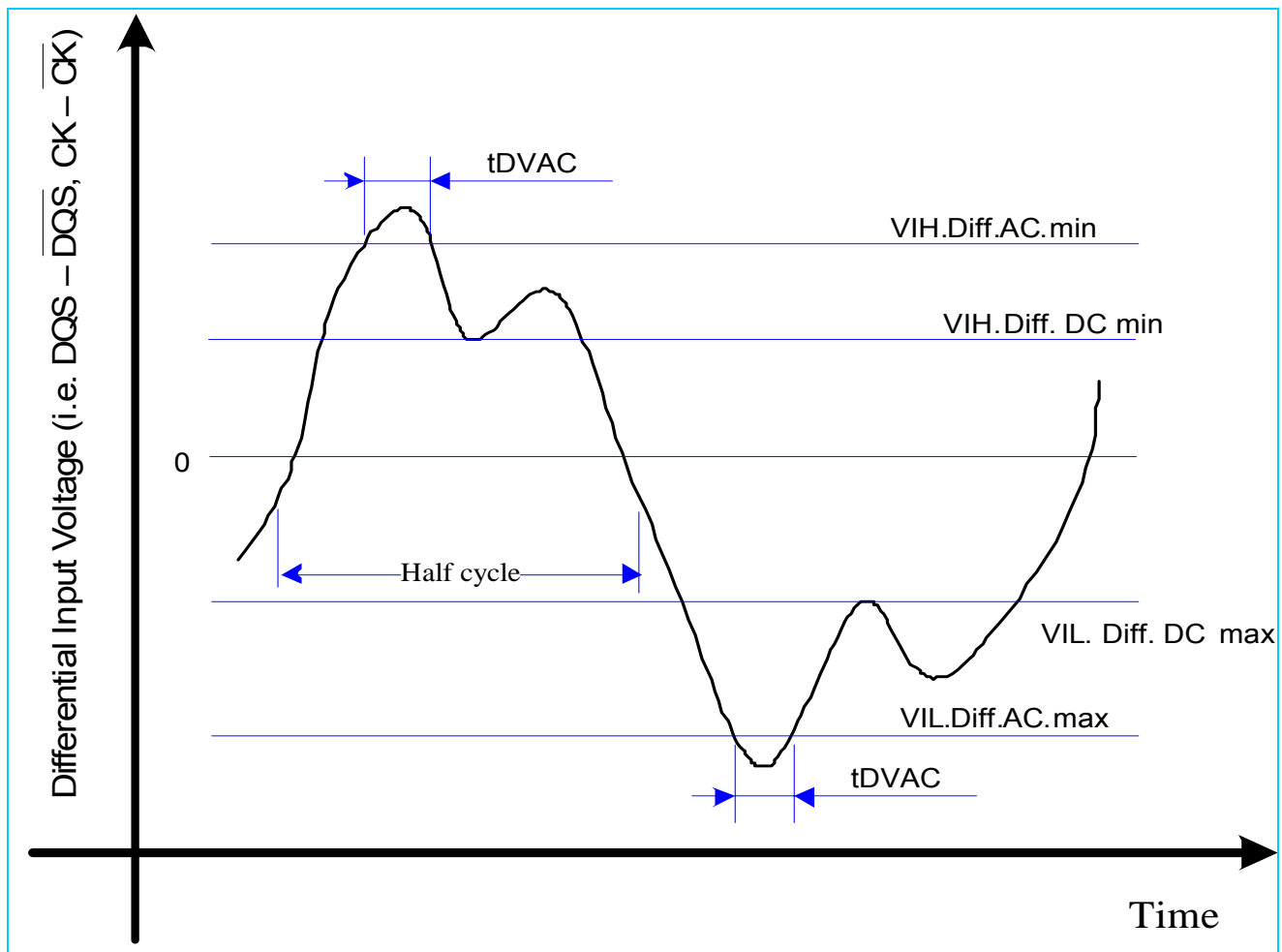
AC and DC Output Measurement Levels

Table 35: Single Ended AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8xVDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5xVDDQ	V	
VOL(DC)	DC output low measurement level (fro IV curve linearity)	0.2xVDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT+0.1xVDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT-0.1xVDDQ	V	1

Note:

1. The swing of ± 0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2.

Table 36: Differential AC and DC Output Levels

Symbol	Parameter	DDR3	Unit	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

Note:

1. The swing of $\pm$ 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT=VDDQ/2 at each of the differential outputs.

Table 37: Single Ended Output Slew Rate

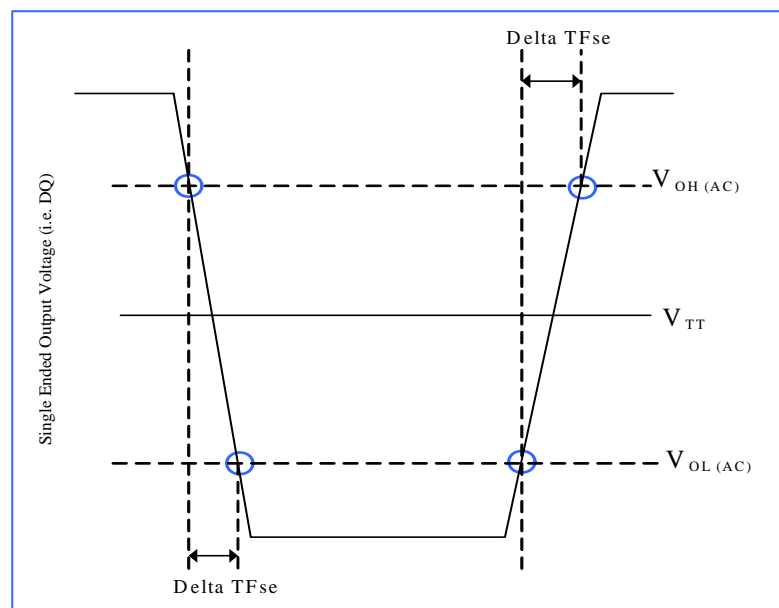| Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC)-VOL(AC)] / DeltaTRse
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC)-VOL(AC)] / DeltaTFse
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			

Fig. 65: Single Ended Output Slew Rate Definition

Table 38: Output Slew Rate (single-ended)

Parameter	Symbol	Operation Voltage	DDR3-1066		DDR3-1333								Unit
			Min.	Max.	Min.	Max.							
Single-ended Output Slew Rate	SRQse	1.35V	1.75	5	1.75	5							V/ns
		1.5V	2.5	5	2.5	5							

Note:

SR: Slew Rate.

Q: Query Output (like in DQ, which stands for Data-in, Query -Output).

se: Single-ended signals.

For Ron = RZQ/7 setting.

Note 1): In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high)

while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high)

while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

Table 39: Differential Output Slew Rate

| Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)] / DeltaTFdiff
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			

Fig. 66: Differential Output Slew Rate Definition
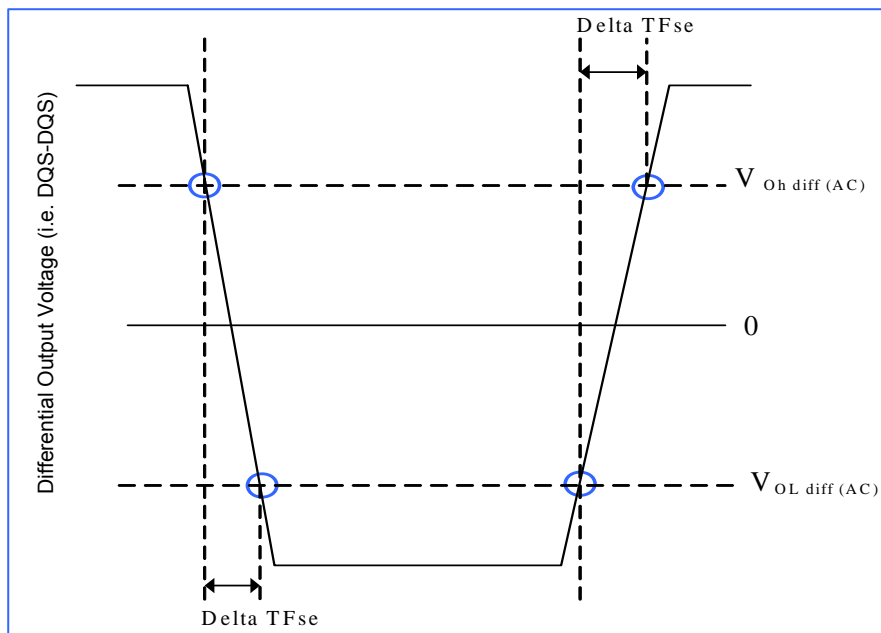
Table 40: Differential Output Slew Rate

Parameter	Symbol	Operation Voltag	DDR3-1066		DDR3-1333								Unit
			Min.	Max.	Min.	Max.							
Single-ended Output Slew Rate	SRQse	1.35V	3.5	12	3.5	12							V/ns
		1.5V	5	10	5	10							
Note:													
SR: Slew Rate.													
Q: Query Output (like in DQ, which stands for Data-in, Query -Output).													
diff: Differential signals.													
For Ron = RZQ/7 setting.													

Reference Load for AC Timing and Output Slew Rate

The following figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.
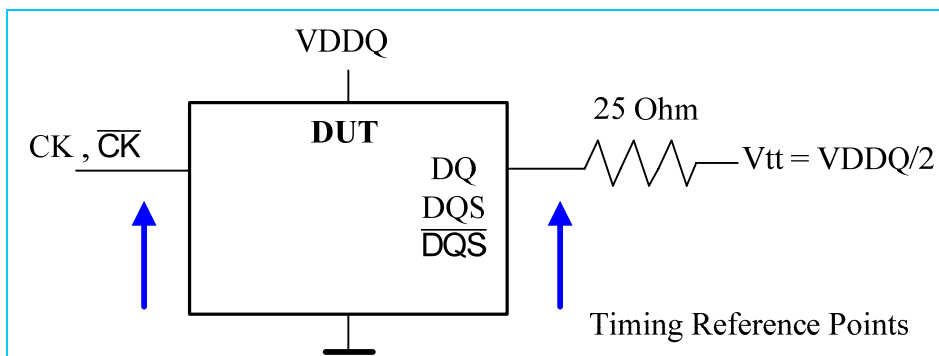
Overshoot and Undershoot Specifications

Table 41: AC Overshoot/Undershoot Specification for Address and Control Pins

Item	DDR3-1066	DDR3-1333				Units
1.35V						
Maximum peak amplitude allowed for overshoot area	TBD	TBD				V
Maximum peak amplitude allowed for undershoot area	TBD	TBD				V
Maximum overshoot area above VDD	TBD	TBD				V-ns
Maximum undershoot area below VSS	TBD	TBD				V-ns
1.5V						
Maximum peak amplitude allowed for overshoot area	0.4	0.4				V
Maximum peak amplitude allowed for undershoot area	0.4	0.4				V
Maximum overshoot area above VDD	0.5	0.4				V-ns
Maximum undershoot area below VSS	0.5	0.4				V-ns
(A0-A13, BA0-BA3, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT)						

Table 42: AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask

Item	DDR3-1066	DDR3-1333				Units
1.35V						
Maximum peak amplitude allowed for overshoot area	TBD	TBD				V
Maximum peak amplitude allowed for undershoot area	TBD	TBD				V
Maximum overshoot area above VDD	TBD	TBD				V-ns
Maximum undershoot area below VSS	TBD	TBD				V-ns
1.5V						
Maximum peak amplitude allowed for overshoot area	0.4	0.4				V
Maximum peak amplitude allowed for undershoot area	0.4	0.4				V
Maximum overshoot area above VDD	0.19	0.15				V-ns
Maximum undershoot area below VSS	0.19	0.15				V-ns
(CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$, DM)						
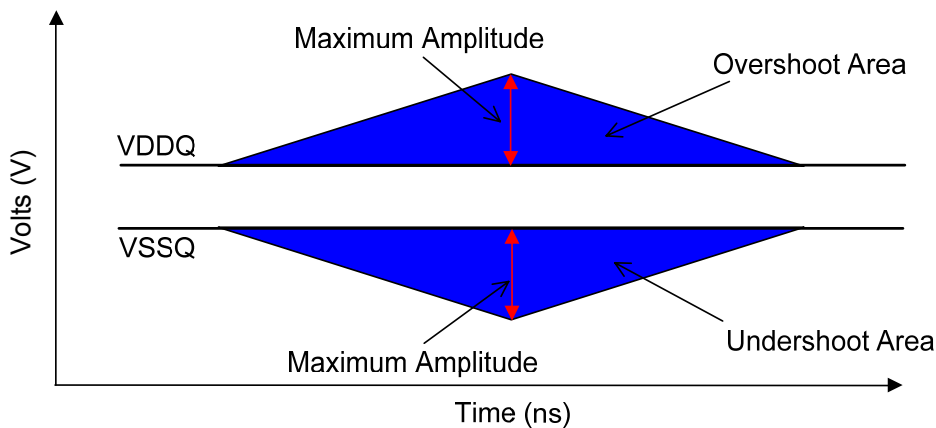
34 Ohm Output Driver DC Electrical Characteristics

A Functional representation of the output buffer is shown as below. Output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:

$RON_{34} = R_{ZQ} / 7$ (nominal 34.4ohms +/-10% with nominal R_{ZQ}=240ohms)

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$RON_{Pu} = [VDDQ-Vout] / | Iout |$ ------------------ under the condition that RON_{Pd} is turned off (1)

$RON_{Pd} = Vout / | Iout |$ ------------------------------under the condition that RON_{Pu} is turned off (2)

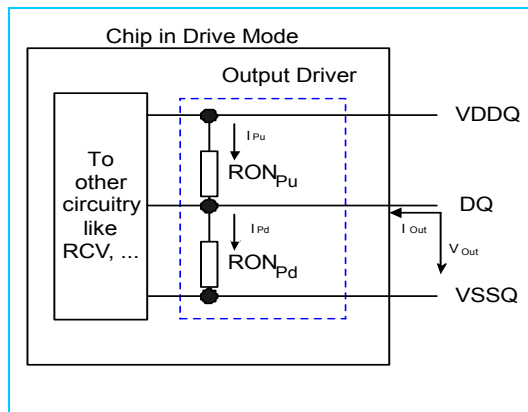## Fig. 67: Output Driver: Definition of Voltages and Currents

Table 43: Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240ohms; entire operating temperature range; after proper ZQ calibration

RON$_{Nom}$	Resistor	Vout	Min.	Nom.	Max.	Unit	Notes
1.35V							
34 ohms	RON$_{34Pd}$	VOLdc = 0.2 x VDDQ	0.6	1.0	1.15	R$_{ZQ}$ / 7	1,2,3
		VOMdc = 0.5 x VDDQ	0.9	1.0	1.15	R$_{ZQ}$ / 7	1,2,3
		VOHdc = 0.8 x VDDQ	0.9	1.0	1.45	R$_{ZQ}$ / 7	1,2,3
	RON$_{34Pu}$	VOLdc = 0.2 x VDDQ	0.9	1.0	1.45	R$_{ZQ}$ / 7	1,2,3
		VOMdc = 0.5 x VDDQ	0.9	1.0	1.15	R$_{ZQ}$ / 7	1,2,3
		VOHdc = 0.8 x VDDQ	0.6	1.0	1.15	R$_{ZQ}$ / 7	1,2,3
40 ohms	RON$_{40pd}$	V_{OLdc} = 0.2 × V_{DDQ}	0.6	1.0	1.15	R$_{ZQ}$ / 6	1,2,3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.15	R$_{ZQ}$ / 6	1,2,3
		V_{OHdc} = 0.8 × V_{DDQ}	0.9	1.0	1.45	R$_{ZQ}$ / 6	1,2,3
	RON$_{40pu}$	V_{OLdc} = 0.2 × V_{DDQ}	0.9	1.0	1.45	R$_{ZQ}$ / 6	1,2,3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.15	R$_{ZQ}$ / 6	1,2,3
		V_{OHdc} = 0.8 × V_{DDQ}	0.6	1.0	1.15	R$_{ZQ}$ / 6	1,2,3
Mismatch between pull-up and pull-down, MM$_{PuPd}$		V$_{OMdc}$ = 0.5 x VDDQ	-10		+10	%	1,2,4

1.5V							
34 ohms	RON$_{34Pd}$	VOLdc = 0.2 x VDDQ	0.6	1.0	1.1	R$_{ZQ}$ / 7	1,2,3
		VOMdc = 0.5 x VDDQ	0.9	1.0	1.1	R$_{ZQ}$ / 7	1,2,3
		VOHdc = 0.8 x VDDQ	0.9	1.0	1.4	R$_{ZQ}$ / 7	1,2,3
	RON$_{34Pu}$	VOLdc = 0.2 x VDDQ	0.9	1.0	1.4	R$_{ZQ}$ / 7	1,2,3
		VOMdc = 0.5 x VDDQ	0.9	1.0	1.1	R$_{ZQ}$ / 7	1,2,3
		VOHdc = 0.8 x VDDQ	0.6	1.0	1.1	R$_{ZQ}$ / 7	1,2,3
40 ohms	RON$_{40pd}$	VOLdc = 0.2 × VDDQ	0.6	1.0	1.1	R$_{ZQ}$ / 6	1,2,3
		VOMdc = 0.5 × VDDQ	0.9	1.0	1.1	R$_{ZQ}$ / 6	1,2,3
		VOHdc = 0.8 × VDDQ	0.9	1.0	1.4	R$_{ZQ}$ / 6	1,2,3
	RON$_{40pu}$	V_{OLdc} = 0.2 × V_{DDQ}	0.9	1.0	1.4	R$_{ZQ}$ / 6	1,2,3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R$_{ZQ}$ / 6	1,2,3
		V_{OHdc} = 0.8 × V_{DDQ}	0.6	1.0	1.1	R$_{ZQ}$ / 6	1,2,3
Mismatch between pull-up and pull-down, MM$_{PuPd}$		V$_{OMdc}$ = 0.5 x VDDQ	-10		+10	%	1,2,4

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.

3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above. e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.

4. Measurement definition for mismatch between pull-up and pull-down, MM$_{PuPd}$:

Measure RONPu and RONPd, but at 0.5 x VDDQ:

MM$_{PuPd}$ = [RONPu - RONPd] / RONNom x 100

Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.

Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

Note: $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

Table 44: Output Driver Sensitivity Definition

Items	Min.	Max.	Unit
RONPU@VOHdc	$0.6 - dR_{ON}dTH*|Delta\ TI - dR_{ON}dVH*|Delta\ VI$	$1.1 + dR_{ON}dTH*|Delta\ TI - dR_{ON}dVH*|Delta\ VI$	$R_{ZQ}/7$
RON@VOMdc	$0.9 - dR_{ON}dTM*|Delta\ TI - dR_{ON}dVM*|Delta\ VI$	$1.1 + dR_{ON}dTM*|Delta\ TI - dR_{ON}dVM*|Delta\ VI$	$R_{ZQ}/7$
RONPD@VOLdc	$0.6 - dR_{ON}dTL*|Delta\ TI - dR_{ON}dVL*|Delta\ VI$	$1.1 + dR_{ON}dTL*|Delta\ TI - dR_{ON}dVL*|Delta\ VI$	$R_{ZQ}/7$

Table 45: Output Driver Voltage and Temperature Sensitivity

Speed Bin	DDR3-1066/1333				Unit
Items	Min.	Max			
dRONdTM	0	1.5			%/°C
dRONdVM	0	0.15			%/mV
dRONdTM	0	1.5			%/°C
dRONdVL	0	0.15			%/mV
dRONdTH	0	1.5			%/°C
dRONdVH	0	0.15			%/mV

Note: These parameters may not be subject to production test. They are verified by design and characterization.

On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6, and A2 of the MR1 Register.

ODT is applied to the DQ, DM, DQS/$\overline{\text{DQS}}$, and TDQS/$\overline{\text{TDQS}}$ (x8 devices only) pins.

A functional representation of the on-die termination is shown in the following figure. The individual pull-up and pull-down resistors (RTT$_{Pu}$ and RTT$_{Pd}$) are defined as follows:

RTT$_{Pu}$ = [VDDQ - Vout] / I Iout I ----------------- under the condition that RTT$_{Pd}$ is turned off (3)

RTT$_{Pd}$ = Vout / I Iout I ---------------------------- under the condition that RTT$_{Pu}$ is turned off (4)

Fig. 68: On-Die Termination: Definition of Voltages and Currents
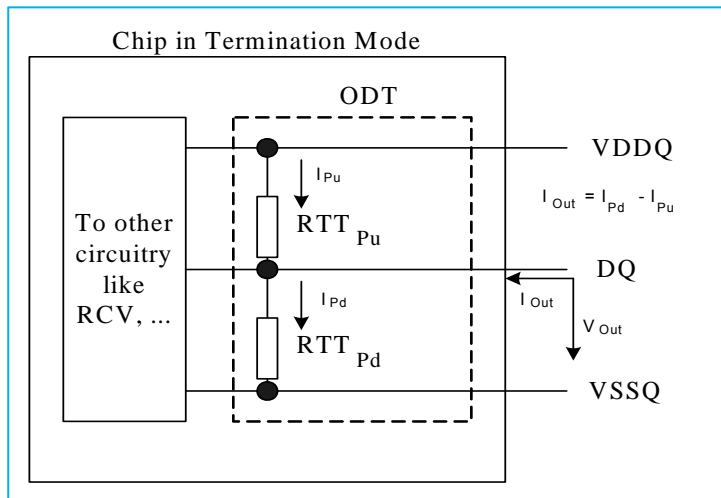
ODT DC Electrical Characteristics

The following table provides an overview of the ODT DC electrical characteristics. The values for RTT$_{60Pd120}$, RTT$_{60Pu120}$, RTT$_{120Pd240}$, RTT$_{120Pu240}$, RTT$_{40Pd80}$, RTT$_{40Pu80}$, RTT$_{30Pd60}$, RTT$_{30Pu60}$, RTT$_{20Pd40}$, RTT$_{20Pu40}$ are not specification requirements, but can be used as design guide lines:

Table 46: ODT DC Electrical Characteristics, assuming R$_{ZQ}$ = 240ohms +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9,A6,A2	RTT	Resistor	Vout	Min.	Nom.	Max.	Unit	Notes
1.35V								
0,1,0	120Ω	RTT120Pd240	VOLdc = 0.2 x VDDQ	0.6	1	1.15	R$_{ZQ}$	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.45	R$_{ZQ}$	1,2,3,4
		RTT120Pu240	VOLdc = 0.2 x VDDQ	0.9	1	1.45	R$_{ZQ}$	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.15	R$_{ZQ}$	1,2,3,4
		RTT120	VIL(ac) to VIH(ac)	0.9	1	1.65	R$_{ZQ}$ /2	1,2,5
0, 0, 1	60Ω	RTT60Pd120	VOLdc = 0.2 x VDDQ	0.6	1	1.15	R$_{ZQ}$/2	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.45	R$_{ZQ}$/2	1,2,3,4
		RTT60Pu120	VOLdc = 0.2 x VDDQ	0.9	1	1.45	R$_{ZQ}$/2	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.15	R$_{ZQ}$/2	1,2,3,4
		RTT60	VIL(ac) to VIH(ac)	0.9	1	1.65	R$_{ZQ}$/4	1,2,5
0, 1, 1	40Ω	RTT40Pd80	VOLdc = 0.2 x VDDQ	0.6	1	1.15	R$_{ZQ}$/3	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.45	R$_{ZQ}$/3	1,2,3,4
		RTT40Pu80	VOLdc = 0.2 x VDDQ	0.9	1	1.45	R$_{ZQ}$/3	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.15	R$_{ZQ}$/3	1,2,3,4
		RTT40	VIL(ac) to VIH(ac)	0.9	1	1.65	R$_{ZQ}$/6	1,2,5
1, 0, 1	30Ω	RTT30Pd60	VOLdc = 0.2 x VDDQ	0.6	1	1.15	R$_{ZQ}$/4	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.45	R$_{ZQ}$/4	1,2,3,4
		RTT30Pu60	VOLdc = 0.2 x VDDQ	0.9	1	1.45	R$_{ZQ}$/4	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.15	R$_{ZQ}$/4	1,2,3,4
		RTT30	VIL(ac) to VIH(ac)	0.9	1	1.65	R$_{ZQ}$/8	1,2,5
1, 0, 0	20Ω	RTT20Pd40	VOLdc = 0.2 x VDDQ	0.6	1	1.15	R$_{ZQ}$/6	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.45	R$_{ZQ}$/6	1,2,3,4
		RTT20Pu40	VOLdc = 0.2 x VDDQ	0.9	1	1.45	R$_{ZQ}$/6	1,2,3,4
			0.5 x VDDQ	0.9	1	1.15	R$_{ZQ}$/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.15	R$_{ZQ}$/6	1,2,3,4
		RTT20	VIL(ac) to VIH(ac)	0.9	1	1.65	R$_{ZQ}$/12	1,2,5
Deviation of VM w.r.t. VDDQ/2, DVM				-5		+5	%	1,2,5,6

MR1 A9,A6,A2	RTT	Resistor	Vout	Min.	Nom.	Max.	Unit	Notes
			1.5V					
0,1,0	120Ω	RTT120Pd240	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}	1,2,3,4
		RTT120Pu240	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}	1,2,3,4
			0.5 x VDDQ	0.9	1	1,1	R_{ZQ}	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}	1,2,3,4
		RTT120	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ} /2	1,2,5
0, 0, 1	60Ω	RTT60Pd120	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}/2	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}/2	1,2,3,4
		RTT60Pu120	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}/2	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}/2	1,2,3,4
		RTT60	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ}/4	1,2,5
0, 1, 1	40Ω	RTT40Pd80	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}/3	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}/3	1,2,3,4
		RTT40Pu80	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}/3	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}/3	1,2,3,4
		RTT40	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ}/6	1,2,5
1, 0, 1	30Ω	RTT30Pd60	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}/4	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}/4	1,2,3,4
		RTT30Pu60	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}/4	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}/4	1,2,3,4
		RTT30	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ}/8	1,2,5
1, 0, 0	20Ω	RTT20Pd40	VOLdc = 0.2 x VDDQ	0.6	1	1.1	R_{ZQ}/6	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1	1.4	R_{ZQ}/6	1,2,3,4
		RTT20Pu40	VOLdc = 0.2 x VDDQ	0.9	1	1.4	R_{ZQ}/6	1,2,3,4
			0.5 x VDDQ	0.9	1	1.1	R_{ZQ}/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1	1.1	R_{ZQ}/6	1,2,3,4
		RTT20	VIL(ac) to VIH(ac)	0.9	1	1.6	R_{ZQ}/12	1,2,5
Deviation of VM w.r.t. VDDQ/2, DVM				-5		+5	%	1,2,5,6

IDD Specifications and Measurement Conditions

Table 52: IDD Specifications (x8)

Symbol	Parameter/Condition	Operation Voltage	DDR3-1066		DDR3-1333								Unit
			Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
IDD0	Operating Current 0 -> One Bank Activate-> Precharge	1.5V	50	56	53	59							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD1	Operating Current 1 -> One Bank Activate-> Read-> Precharge	1.5V	67	74	71	79							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	1.5V	5	9	5	9							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	1.5V	16	20	18	22							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD2Q	Precharge Quiet Standby Current	1.5V	25	31	28	35							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD2N	Precharge Standby Current	1.5V	26	32	30	35							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD3P	Active Power-Down Current Always Fast Exit	1.5V	16	21	19	23							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD3N	Active Standby Current	1.5V	29	35	32	38							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD4R	Operating Current Burst Read	1.5V	97	106	113	122							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD4W	Operating Current Burst Write	1.5V	94	104	109	119							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD5B	Burst Refresh Current	1.5V	47	52	50	55							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD6	Self-Refresh Current Normal Temperature Range (0-85°C)	1.5V	3	7	3	7							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD6ET	Self-Refresh Current: extended temperature range	1.5V	4	8	4	8							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD6TC	Auto Self-Refresh Current	1.5V	4	8	4	8							mA
		1.35V	TBD	TBD	TBD	TBD							
IDD7	All Bank Interleave Read Current	1.5V	169	184	203	220							mA
		1.35V	TBD	TBD	TBD	TBD							

IDD Specifications and Measurement Conditions

Table 53: IDD Specifications (x16)

Symbol	Parameter/Condition	Operation Voltage	DDR3-1066 Typ.	DDR3-1066 Max.	DDR3-1333 Typ.	DDR3-1333 Max.							Unit
IDD0	Operating Current 0 -> One Bank Activate-> Precharge	1.5V	63	76	66	80							mA
		1.35V	59	69	65	76							
IDD1	Operating Current 1 -> One Bank Activate-> Read-> Precharge	1.5V	87	106	92	112							mA
		1.35V	79	93	85	100							
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	1.5V	5	12	5	13							mA
		1.35V	3.4	8	3.4	10							
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	1.5V	16	21	18	23							mA
		1.35V	16	21	18	23							
IDD2Q	Precharge Quiet Standby Current	1.5V	26	31	29	34							mA
		1.35V	25	31	29	34							
IDD2N	Precharge Standby Current	1.5V	27	33	30	35							mA
		1.35V	26	33	30	35							
IDD3P	Active Power-Down Current Always Fast Exit	1.5V	17	25	20	27							mA
		1.35V	17	25	20	27							
IDD3N	Active Standby Current	1.5V	29	38	33	41							mA
		1.35V	28	38	32	40							
IDD4R	Operating Current Burst Read	1.5V	132	165	157	195							mA
		1.35V	111	133	132	158							
IDD4W	Operating Current Burst Write	1.5V	130	162	152	189							mA
		1.35V	119	129	141	154							
IDD5B	Burst Refresh Current	1.5V	48	56	51	59							mA
		1.35V	45	51	49	56							
IDD6	Self-Refresh Current Normal Temperature Range (0-85°C)	1.5V	4	7	4	7							mA
		1.35V	2	7	2	7							
IDD6ET	Self-Refresh Current: extended temperature range	1.5V	4	8	4	8							mA
		1.35V	2	8	2	8							
IDD6TC	Auto Self-Refresh Current	1.5V	4	8	4	8							mA
		1.35V	2	8	2	8							
IDD7	All Bank Interleave Read Current	1.5V	212	266	236	297							mA
		1.35V	191	230	222	267							

Table 54: IDD Measurement Conditions

Symbol	Parameter/Condition
IDD0	Operating Current - One bank Active - Precharge current CKE: High; External clock: On; tCK, tRC, tRAS: see table in the next page; CS: High between ACT and PRE; Command Inputs: SWITCHING[1] (except for ACT and PRE); Row, Column Address, Data I/O: SWITCHING1 (A10 Low permanently); Bank Address: fixed (Bank 0); Output Buffer: off[2]; ODT: disabled[3]; Active Banks: one (ACT-PRE loop); Idle Banks: all other; Pattern example: A0 D DD DD DD DD DD DD D P0.[4]
IDD1	Operating One bank Active-Read-Precharge Current CKE: High; External clock: On; tCK, tRC, tRAS, tRCD, CL, AL: see table in the next page; CS: High between ACT, RD, and PRE; Command Inputs: SWITCHING[1] (except ACT, RD, and PRE Commands); Row, Column Address: SWITCHING1 (A10 Low permanently); Bank Address: fixed (Bank 0); Data I/O: switching every clock (RD Data stable during one Clock cycle); floating when no burst activity; Output Buffer: Off[2]; ODT: disabled[3]; Burst Length: BL85; Active Banks: one (ACT-RD-PRE loop); Idle Banks: all other; Pattern example: A0 D DD D R0 DD DD DD DD D P0[4].
IDD2N	Precharge Standby Current CKE=High; External Clock=On; tCK: see table in the next page; CS: High; Command Inputs, Row, Column, Bank Address, Data I/O: SWITCHING[1]; Output Buffer: Off[2]; ODT: disabled[3]; Active / Idle Banks: none / all.
IDD2P(0)	Precharge Power-Down Current - (Slow Exit) CKE=Low; External Clock=On; tCK: see table in the next page; CS: Stable; Command Inputs: Stable; Row, Column / Bank Address: Stable; Data I/O: floating; Output Buffer: Off[2]; ODT: disabled[3]; Active / Idle Banks: none / all. Precharge Power Down Mode: Slow Exit[6] (RD and ODT must satisfy tXPDLL - AL)
IDD2P(1)	Precharge Power-Down Current - (Fast Exit) CKE=Low; External Clock=On; tCK: see table in the next page; CS: Stable; Command Inputs, Row, Column, Bank Address: Stable; Data I/O: floating; Output Buffer: Off[2]; ODT: disabled[3]; Active / Idle Banks: none / all. Precharge Power Down Mode: Fast Exit 6(any valid Command after tXP)[7]
IDD2Q	Precharge Quiet Standby Current CKE=High; External Clock=On; tCK: see table in the next page; CS=High; Command Inputs, Row, Column, Bank Address: Stable; Data I/O: floating; Output Buffer: Off2; ODT: disabled[3]; Active / Idle Banks: none / all.
IDD3N	Active Standby Current CKE=High; External Clock=On; tCK: see table in the next page; CS=High; Command Inputs, Row, Column, Bank Address, Data I/O: SWITCHING[1]; Output Buffer: Off2; ODT: disabled[3]; Active / Idle Banks: All / none.
IDD3P	Active Power-Down Current CKE=Low; External Clock=On; tCK: see table in the next page; CS, Command Inputs, Row, Column, Bank Address: Stable; Data I/O: floating; Output Buffer: Off2; ODT: disabled[3]; Active / Idle Banks: All / none.
IDD4R	Operating Burst Read Current CKE=High; External Clock=On; tCK, CL: see table in the next page; AL: 0; CS: High between valid Commands; Command Inputs: SWITCHING[1] (except RD Commands); Row, Column Address: SWITCHING[1] (A10: Low permanently); Bank Address: cycling[10]; Data I/O: Seamless Read Data Burst : Output Data switches every clock cycle (i.e. data stable during one clock cycle); Output Buffer: Off[2]; ODT: disabled[3]; Burst Length: BL8[5]; Active / Idle Banks: All / none[10]; Pattern: R0 D DD R1 D DD R2 D DD R3 D DD R4[4]
IDD4W	Operating Burst Write Current CKE=High; External Clock=On; tCK, CL: see table in the next page; AL: 0; CS: High between valid Commands; Command Inputs: SWITCHING[1] (except WR Commands); Row, Column Address: SWITCHING[1] (A10: Low permanently); Bank Address: cycling[10]; Data I/O: Seamless Write Data Burst : Input Data switches every clock cycle (i.e. data stable during one clock cycle); DM: L permanently; Output Buffer: Off[2]; ODT: disabled[3]; Burst Length: BL8[5]; Active / Idle Banks: All / none[10]; Pattern: W0 D DD W1 D DD W2 D DD W3 D DD W4[4]
IDD5B	Burst Refresh Current CKE=High; External Clock=On; tCK, tRFC: see table in the next page; CS: High between valid Commands; Command Inputs, Row, Column, Bank Addresses, Data I/O: SWITCHING[1]; Output Buffer: Off[2]; ODT: disabled[3]; Active Banks: Refresh Command every tRFC=tRFC(IDD); Idle banks: none.
IDD6	Self-Refresh Current Tcase=0-85°C; Auto Self Refresh =Disable; Self Refresh Temperature Range=Normal[9]; CKE=Low; External Clock=Off (CK and CK: Low); CS, Command Inputs, Row, Column Address, Bank Address, Data I/O: Floating; Output Buffer: off[2]; ODT: disabled[3]; Active Banks: All (during Self-Refresh action); Idle Banks: all (between Self-Rerefresh actions)
IDD6ET	Self-Refresh Current: extended temperature range Tcase=0-95°C; Auto Self Refresh =Disable; Self Refresh Temperature Range=Extended[9]; CKE=Low; External Clock=Off (CK and CK: Low); CS, Command Inputs, Row, Column Address, Bank Address, Data I/O: Floating; Output Buffer: off[2]; ODT: disabled[3]; Active Banks: All (during Self-Refresh action); Idle Banks: all (between Self-Rerefresh actions)

IDD6TC	Auto Self-Refresh Current Tcase=0-95°C; Auto Self Refresh =Enable[8]; Self Refresh Temperature Range=Normal[9]; CKE=Low; External Clock=Off (CK and CK: Low); CS, Command Inputs, Row, Column Address, Bank Address, Data I/O: Floating; Output Buffer: off [2]; ODT: disabled [3]; Active Banks: All (during Self-Refresh action); Idle Banks: all (between Self-Rerefresh actions)
IDD7	Operating Bank Interleave Read Current CKE=High; External Clock=On; tCK, tRC, tRAS, tRCD, tRRD, CL: see table as below; AL=tRCD.min-tCK; CS=High between valid commands; Command Input: see table; Row, Column Address: Stable during DESELECT; Bank Address: cycling[10]; Data I/O: Read Data: Output Data switches every clock cycle (i.e. data stable during one clock cycle); Output Buffer: Off [2];ODT: disabled [3]; Burst Length: BL8; Active / Idle Banks: All [10] / none.

Note1: SWITCHING for Address and Command Input Signals as described in Definition of SWITCHING for Address and Command Input Signals Table.
Note2: Output Buffer off: set MR1 A[12] = 1
Note3: ODT disable: set MR1 A[9,6,2]=000 and MR2 A[10,9]=00
Note4: Definition of D and D: described in Definition of SWITCHING for Address and Command Input Signals Table; Ax/Rx/Wx: Activate/Read/Write to Bank x.
Note5: BL8 fixed by MRS: set MR0 A[1,0]=00
Note6: Precharge Power Down Mode: set MR0 A12=0/1 for Slow/Fast Exit
Note7: Because it is an exit after precharge power down, the valid commands are: ACT, REF, MRS, Enter Self-Refresh.
Note8: Auto Self-Refresh(ASR): set MR2 A6 = 0/1 to disable/enable feature
Note9: Self-Refresh Temperature Range (SRT): set MR2 A7 = 0/1 for normal/extended temperature range
Note10: Cycle banks as follows: 0,1,2,3,...,7,0,1,...

Package Dimensions (x8; 78 balls; 0.8mmx0.8mm Pitch; BGA)

Package Dimensions (x16; 96 balls; 0.8mmx0.8mm Pitch; BGA)

Bottom View

6.40

0.8

0.8

12.00

Min 0.1

Min 0.1

9.00 +/- 0.10

Max. 1.20

Min 0.25
Max 0.40

13.00 +/- 0.10

96 x Ø   Min. 0.40
Max. 0.50